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AUTOMATIC MICROCIRCUIT BRIDGE AND AUTOBALANCING UNIT.(U)
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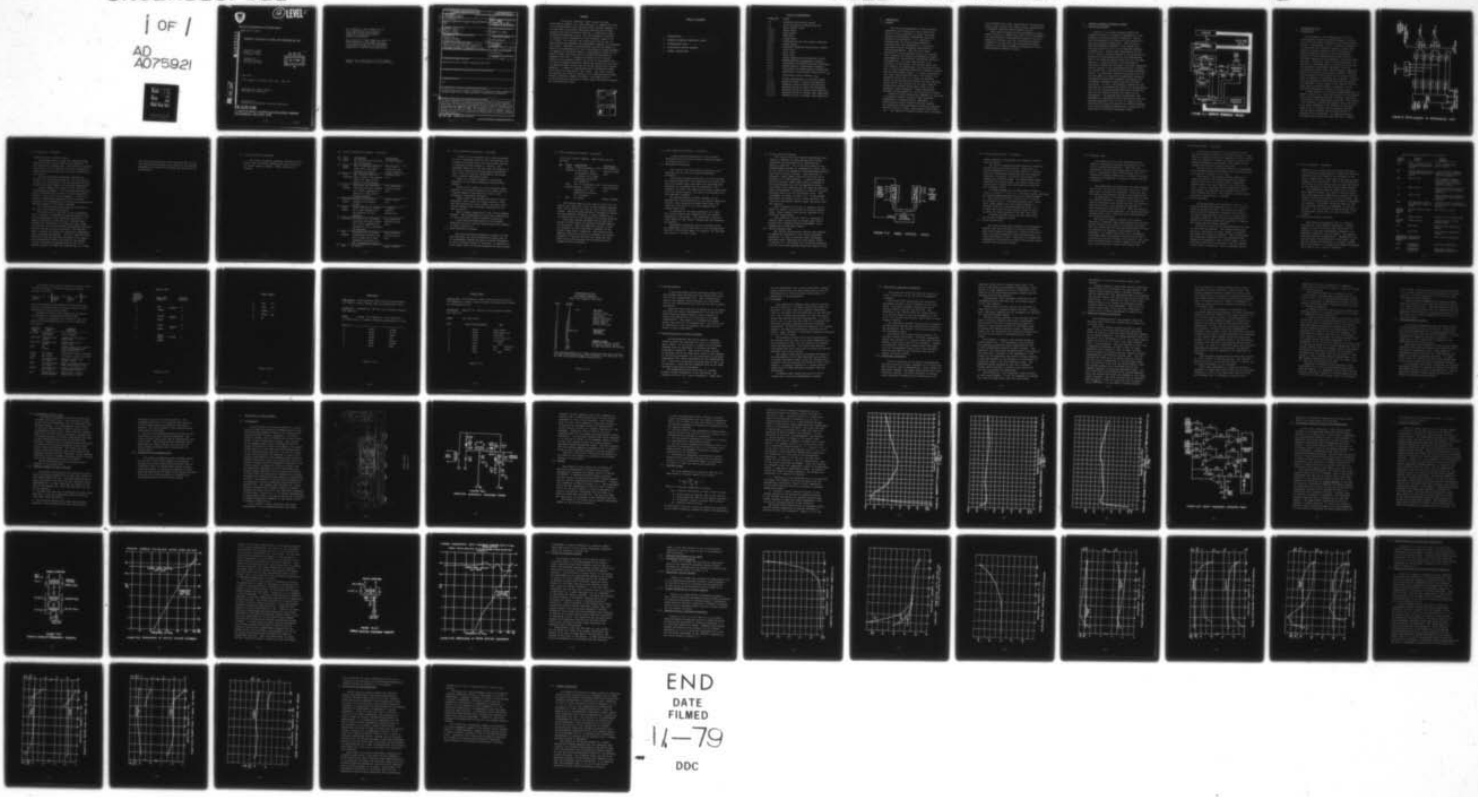

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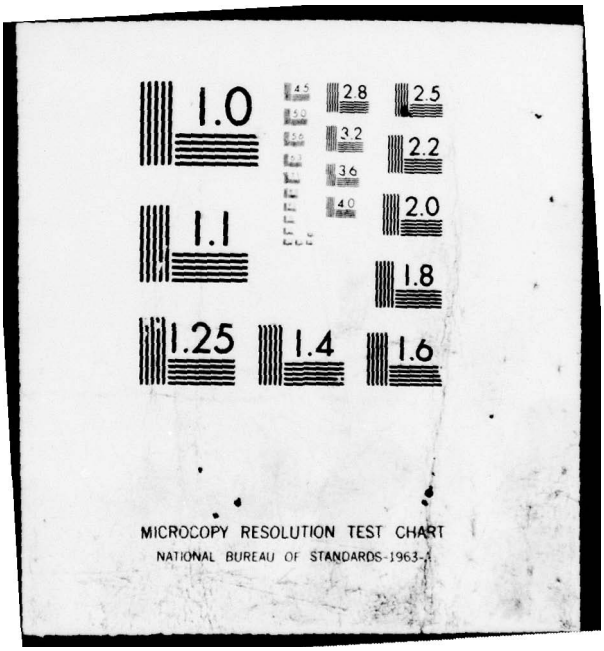
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Research and Development Technical Report

DELET-TR-76-1380-F

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AUTOMATIC MICROCIRCUIT BRIDGE AND AUTOBALANCING UNIT

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Final Report for Period June 1976 - May 1977

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Prepared for:
Electronics Technology & Devices Laboratory

ERADCOM

US ARMY ELECTRONICS RESEARCH AND DEVELOPMENT COMMAND
FORT MONMOUTH, NEW JERSEY 07703

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This report summarizes the design and test of a Microcricuit Bridge and Balancing Unit to be used in a precision measurement of quartz crystal resonators. Design goals for the Bridge and Balancing Unit were to measure resistance with a 5% accuracy and capacitance with a ±.1 pF accuracy from .8 to 220 MHz and at temperatures from -50°C to +105°C. The autobalance Unit will perform initial balance, final balance, and plus/minus susceptance offset on command. Based on the measured data, it will be possible to calculate the Q of the crystal resonator being tested.

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Summary

This final technical report covers the work performed by GenRad, Inc. under Contract No. DAAB07-76-C-1380 on an Autobalancing Unit and Microcircuit Bridge Assembly to be used with a previously developed Tracking Servo Bridge Detector and Local Oscillator System, in combination with a synthesized frequency source, for the automated evaluation of quartz-crystal resonators in the frequency range of 0.8 to 220 MHz. The contract was issued June 1976 by the U.S. Army Electronics Research and Development Command, Fort Monmouth, New Jersey. Research and development work was performed, to design an Autobalancing Unit and a Microcircuit Bridge Assembly to complete an automated system. Developmental models of one each of these units were built by GenRad and delivered to ERADCOM in May 1977. Complete evaluation of the overall system was not possible within the scope of the contract but the basic automated balancing concept was checked out with both a simulated bridge circuit and the actual Microcircuit Bridge Assembly. A number of improvements were indicated by these tests which are discussed in the report. See final reports for previous work done by GenRad on the Tracking Servo Bridge Detector (Contract DAAB07-73-C-0609), and ECOM-75-1341-F on the Microcircuit Bridge and Offset Local Oscillator required for the measuring system.

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1. INTRODUCTION

1.1 General

The accurate measurement of quartz-crystal resonators on a production line or depot-test basis is vitally required in order to provide accurate and precisely reproducible data with production efficiencies. It is generally accepted that the most accurate method of characterizing such resonators is in terms of equivalent-circuit parameters determined by bridge measurements. The fact that these equivalent circuit parameter values vary rapidly with frequency and thermal environment has made measurements by conventional instruments difficult and expensive. For most applications it is necessary to characterize the devices under test as a function of temperature, with negligible error due to interconnections between the measuring circuit and the device being tested. If large corrections for these interconnections are to be avoided, the measuring device must be as small as possible, placed in direct physical contact with the resonator being tested, and subjected to the same range of temperatures without significant effect on the parameter values indicated. These requirements dictated the development of the microcircuit bridge.

GenRad has been working with ERADCOM for some time in creating a modular system to make automatic measurements on quartz-crystal resonators. A tracking servo bridge detector has been readied for production under Production Engineering Measures Contract Project 2739544, specification MIL-D-55361 (EL). The requisite automatic offset local oscillator

was developed and a paper study made of a microcircuit bridge under Contract No. DAAB07-C-1341, Research and Development Technical Report ECOM-75-1341-F.

This report covers the work performed by GenRad under Contract No. DAAB07-76-C-1380 in the development and construction of developmental models of an auto-balancing interface unit and a microcircuit bridge assembly to be used with the previously developed items and a suitable frequency synthesizer to form a demonstratable automatic system.

2. COMPLETE AUTOMATIC MEASURING SYSTEM

2.1 General Description

Figure 2.1 is a block diagram showing the elements required for automatic measurement of the parameters of quartz-crystal resonators. Manual set-up adjustments are entered via the keyboard of the desk calculator/controller. This device is most conveniently connected to the system auto-balancing interface unit via an IEEE 488 standard interface bus. Digital data representing the "R" and "C" control voltages applied to the microcircuit bridge by the autobalancing unit are communicated back to the desk calculator/controller via the IEEE 488 bus. A program stored in the calculator/controller, along with providing the proper sequencing control signals to the autobalancing unit, converts the digital data returned into the desired parameter values. An additional frequency interface unit, not yet developed, is required to communicate frequency information between the frequency synthesizer and incremental frequency counter and the calculator/controller. In fact, the elements required for the IEEE 488 bus interconnection between the autobalancing unit and the calculator/controller were outside the scope of the present contract and remain to be implemented. The demonstration autobalance unit developed is sequenced by panel push buttons and the voltages applied to the "R" and "C" inputs to the microcircuit bridge are read out on digital displays which must be manually entered into a calculator for reduction to the desired parameter values.

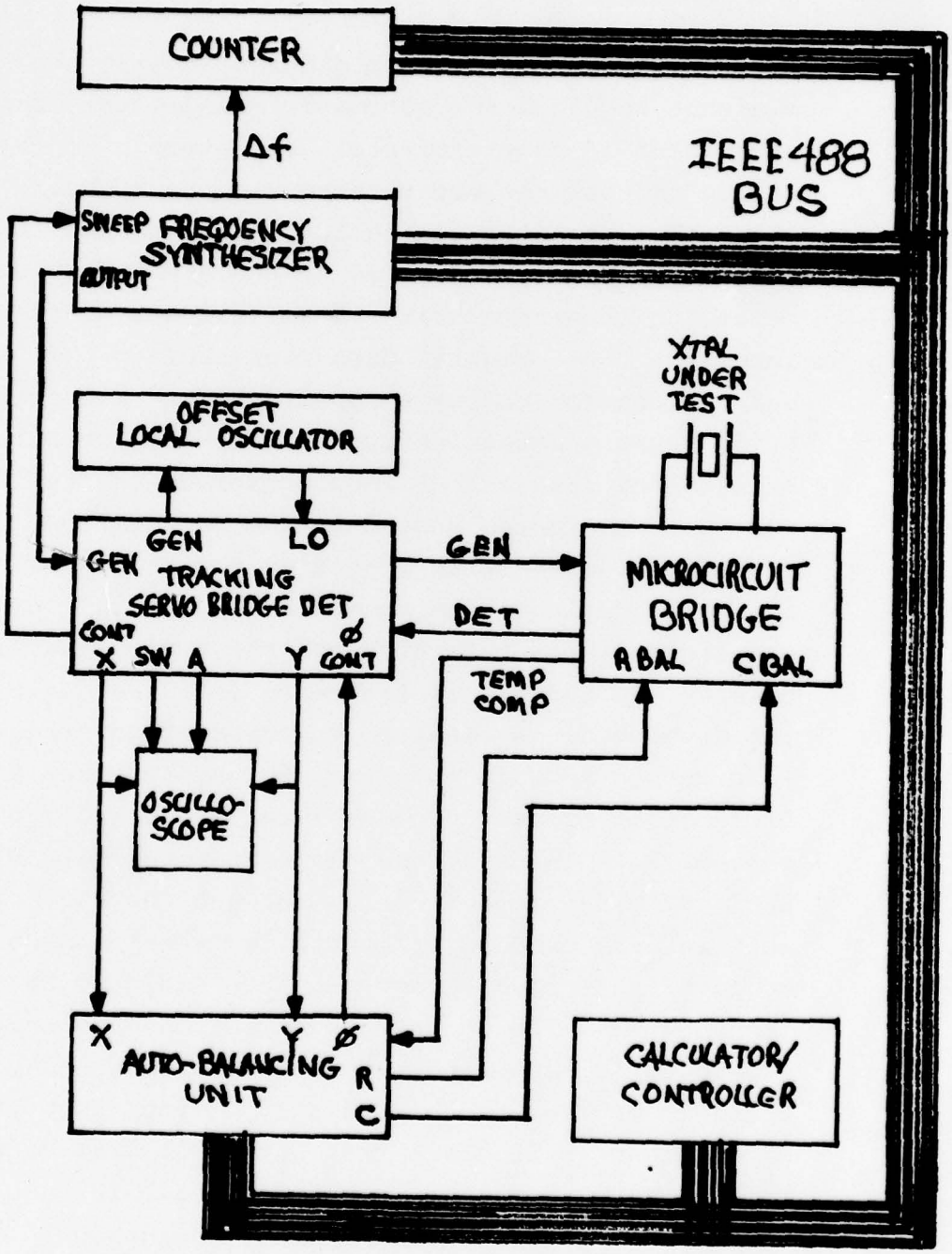


FIGURE 2.1 AUTOMATIC MICROCIRCUIT BRIDGE

3. AUTOBALANCING UNIT

3.1 Introduction

The purpose of the Autobalancing Unit is to automatically perform the steps necessary to effect the initial and final balances of the RF microcircuit bridge. Upon command, the unit executes a sequence of operations that generate signals to adjust the detector reference phase and the two bridge arms using information from the X and Y synchronous detectors of the Tracking Servo Bridge Detector. Two basic operations are performed, initial and final balances. During the initial balance procedure, the detector IF reference phase is adjusted to align the two quadrature synchronous detectors with the corresponding bridge arms, thus providing independent control of resistive and reactive balance. Data are then obtained for each bridge arm at initial balance (when no unknown is connected to the bridge). Similar data are obtained at final balance (when an unknown is connected), and the value of the unknown is determined from calculation based, in essence, on the difference between the initial and final values.

A block diagram of the basic Autobalancing Unit is shown in Figure 3.1. The unit consists of five digital servos with associated digital-to-analog conversion, data routing, and control logic circuits. Each digital servo contains a 3-digit BCD register which can count up or down, depending on the polarity of an analog input signal. Digital data are obtained directly from the servo register and an analog output is obtained by D/A conversion. An important feature of these digital servos is their ability to remain

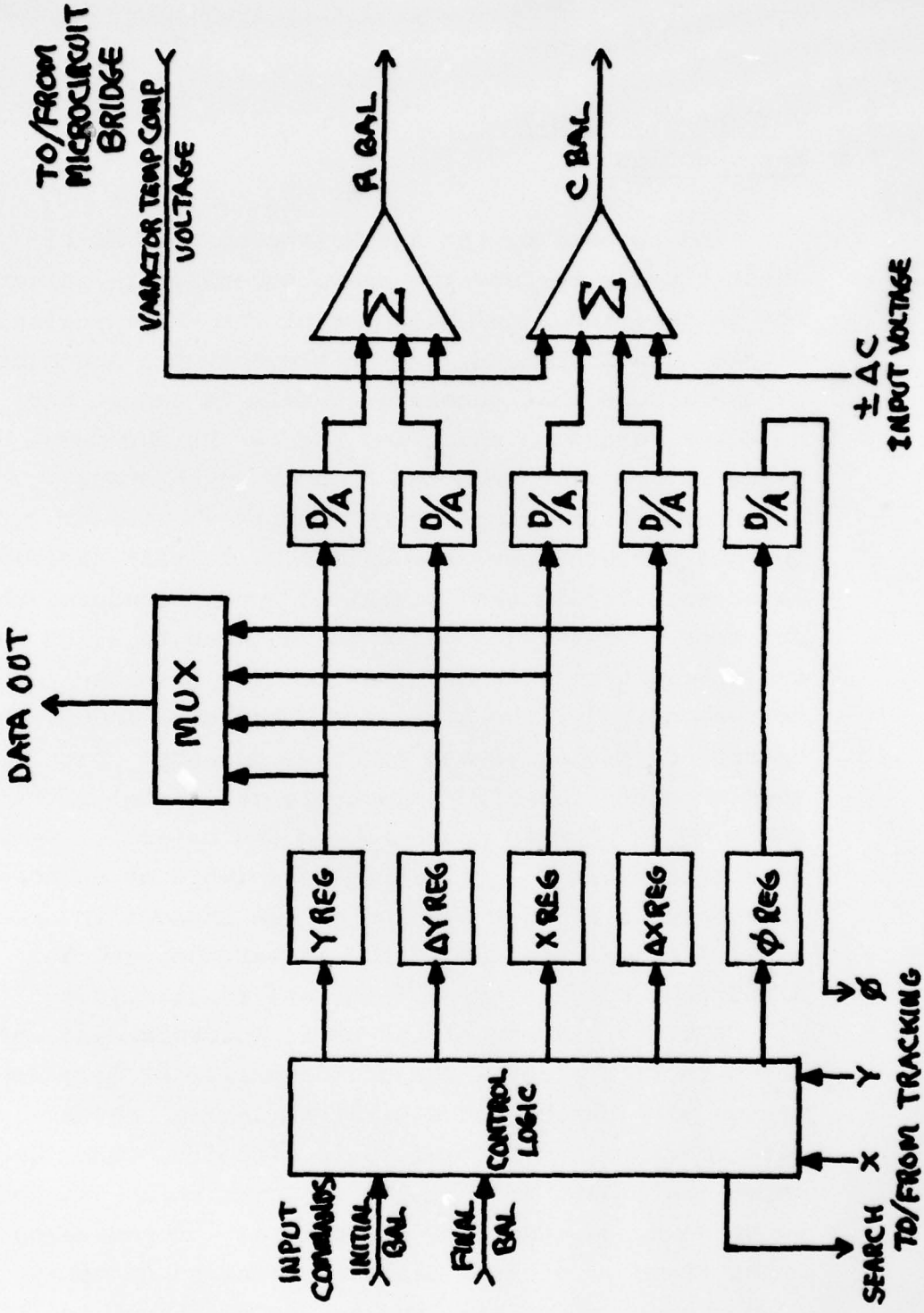


FIGURE 3.1 BLOCK DIAGRAM OF AUTOBALANCING UNIT

3.1 Introduction - continued

indefinitely at a certain value.

One digital servo is used for reference phase (Ø) and two are used for each of the resistive (Y) and reactive (X) bridge arms. The latter are arranged with coarse (X or Y) and fine (ΔX or ΔY) weighting having one digit overlap for an overall resolution of five digits.

The only external information required for operation of the Autobalancing Unit is the polarity of the X and Y detectors. This is obtained from the detector dc output signals by precision comparators.

Control commands are used to start initial or final balance sequences. The final balance operation may be performed with a choice of three capacitive offsets: zero, positive, or negative. Provision is made for temperature compensation of the bridge varactors by an appropriate dc voltage from temperature-sensing elements in the bridge assembly.

Four 3-digit data output words are available at the end of each balancing sequence.

The objectives of this part of the development were to procure a completely automated system to perform the necessary bridge balancing operations in a manner equivalent to that done by a skilled human operator but preferably at a much more rapid speed. An objective of 50 milliseconds per balancing operation was not achieved nor was a setting of the detector phase to within one degree for completely independent R and C balance adjustments. How well these and other objectives were achieved are discussed in the report. Also discussed but beyond the scope of the present contract are means of implementing control of the complete system via IEEE 488 interface bus, by a desk-

top controller/calculator which would provide not only the calculations necessary for readout of the desired parameters, but means for entering the setup data for measurements.

3.2 Initial Balancing Procedure

The initial balancing procedure consists of nine states that are entered sequentially upon receipt of an initial balance command. These states are as follows:

3.2 Initial Balancing Procedure - continued

No.	State	Description	Termination
0	Reset	All counters and registers are initialized.	RC time constant
1	Phase Sweep	The IF reference phase is swept until the proper quadrant is located.	Both X and Y detectors have proper polarity.
2	Phase Increment	The reference phase is swept further from approximately the edge to the center of the quadrant.	Counter carry out.
3	Coarse Balance	Resistance and reactance registers are both clocked up or down, depending on polarity of the corresponding detector.	Both detectors cycling around zero.
4	Reactance Offset	Reactance register is clocked up to produce offset.	Counter carry out.
5	Phase Adjust	Phase register is clocked up or down depending on the polarity of the Y detector.	Y detector cycling around zero.
6	Rebalance	Resistance and reactance registers are both clocked up or down, depending on polarity of the corresponding detector.	Both detectors cycling around zero.
7	Fine Balance	Resistance and reactance interpolate registers are both clocked up or down depending on polarity of the corresponding detector.	Both detectors cycling around zero.
8	Done	No action	Manual command.

3.2 Initial Balancing Procedure - continued

Steps 0-2 are associated with rough adjustment of the IF reference phase so that the detectors are aligned sufficiently well with the bridge arms that a convergent coarse balance is insured. This procedure makes use of the fact that the polarity of the X and Y detectors indicates phase information even if they are grossly overloaded by the signal from a totally unbalanced bridge.

Step 3 is a coarse balance of the bridge, necessary for the phase adjustment process which follows.

Steps 4 and 5 result in a more accurate phase setting. The reactive bridge arm is offset and the reference phase is adjusted for a null of the orthogonal (resistance) detector.

Steps 6 and 7 then perform the actual initial balancing, first using the coarse registers (with the fine registers at their center) and then a more precise balance with the higher resolution of the fine registers.

Step 8 signals completion of the initial balance process. The Autobalance Unit will wait indefinitely in this state until another command is received.

A more detailed description of the hardware associated with the initial balance operations appears in report section 3.6.

3.3 Final Balancing Procedure

The final balancing procedure is similar to that just described for initial balancing, except that it is considerably simpler because no further adjustment of the IF reference phase is required. It consists of three states that are entered sequentially upon receipt

3.3 Final Balancing Procedure - continued

of a final balance command. These states are as follows:

No.	State	Description	Termination
0	Coarse Balance	A search command is sent to the TSBD. The Y (resistance) register is clocked up or down, depending on polarity on Y detector.	Both detectors cycling around zero.
1	Fine Balance	The ΔY (resistance inter polate) register is clocked up or down depending on polarity of Y detector.	Both detectors cycling around zero.
2	Done	No action.	Manual command.

The actions taken by the Y and ΔY servos are the same as for Steps 6-8 of the initial balance procedure. The X and ΔX servos are held at their initial balance states. Reactive bridge balance is obtained by adjusting the generator frequency, a basic capability of the analog servo in the Tracking Servo Bridge Detector.

This final balance procedure can be done with either of three values of capacitive offsets applied to the bridge. When the capacitive offset is zero, the resonant (or zero reactance) frequency of the crystal under test is measured. When positive and negative capacitive offsets are applied, the crystal frequency is "pulled" and data are generated from which the crystal motional arm equivalent circuit elements may be determined.

3.3 Final Balancing Procedure - continued

A more detailed description of the hardware associated with the final balance operations appears in report section 3.7.

3.4 Measurement Procedures

The initial and final balance operations just described can be used for several measurement procedures.

Two initial balance operations, the first without an unknown connected to the bridge and the second with one, can generate data from which the resistance and reactance of the unknown can be determined. This procedure is useful for measuring the static capacitance (C_o) of a quartz crystal, and would be performed at an off-resonance frequency.

An initial balance, without unknown, can be followed by a final balance with and without capacitive offsets. This procedure generates data which can, along with the value of C_o, fully characterize a crystal under test.

A variation of the above procedure is to make the initial balance off-resonance with the crystal connected to the bridge. This technique is particularly useful at VHF, where a balance may not otherwise be possible.

Measurement procedures may be initiated either by pushbuttons on the front panel of the Autobalancing Unit as in the current model, or remotely, as described in Section 3.1 of this report.

3.5 Control Logic Principles

The initial and final balancing procedures each require a sequence of steps during which certain operations are performed until terminated by a specific condition. One of the most powerful, yet understandable methods of implementing control logic of this type is to address a multiplexer/demultiplexer pair from a digital register. Each operation is assigned a state number, which in this case can be arranged in a fixed sequence. A counting register holds the current state number which is decoded by the demultiplexer onto the corresponding control line which is the stimulus for the required operation and the multiplexer is switched to look for a certain condition which will end the current state. This arrangement is shown in Figure 3.5. In the present case where the states are in a fixed sequence, the "look for" multiplexer output clocks the state counting register.

Each "stimulus" line will, in general, drive a number of control lines through an array of gating logic. Other similar logic may be required at the "look for" multiplexer.

This method of control logic is conceptually simpler than a large array of random logic and is particularly convenient during development since changes can be made quite simply.

3.6 Initial Balance Logic

The Initial Balance Logic controls the sequence of operations required for the initial balancing procedure. It uses the control logic principles described above, employing the nine states listed in Section 3.2. The outputs are associated primarily with the five Servo Registers while the inputs to the

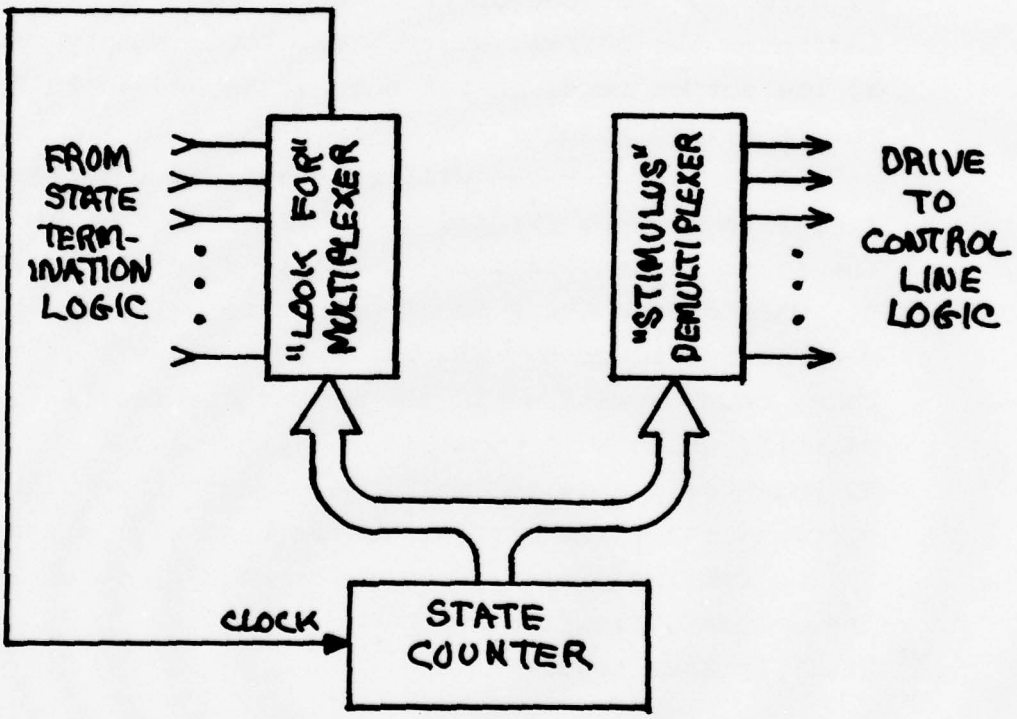


FIGURE 3.5 BASIC CONTROL LOGIC

3.6 Initial Balance Logic - continued

state termination multiplexer are primarily from the Detector Board.

The initial balancing process begins by resetting and activating the state counter. Each state is entered sequentially as the state counter is clocked up by the termination multiplexer when the required condition is reached. The end of the process is signaled by the Done output. An on-board LED display indicates the current state. The logic simply sets up the action required for each state and looks for the necessary result.

A typical example will be described for State 1 (refer to Figures 3.1 and 3.5). The state counter addresses the stimulus demultiplexer and its #1 output becomes H. This causes the Ø count output to go L, and the ø up output to go H. The phase register will, therefore, count upward until the proper quadrant is reached, which will cause the quadrant input to go H, which will make the multiplexer output go high, clocking the state counter to its next (#2) state.

A similar process occurs for each state until the initial balancing is done.

3.7 Final Balance Logic

The Final Balance Logic hardware is considerably simpler than that required for the Initial Balance. Only three states are needed and, since the two active states are both terminated by the balance signal, no state multiplexer is used. Similarly, the operations performed are controlled by simple logic gating driven directly from the state counter.

3.8 Detector Logic

The control logic of the Autobalancing Unit requires information regarding the polarity of the X and Y synchronous detectors. These data are provided by two precision comparators on the Detector Board. The Detector Board also contains logic to indicate the phase quadrant and to indicate a balance condition for either the Y detector or both the X and Y detectors.

The comparators are chosen for low offset voltage (0.8 mV max. at 25°C and 1.4 mV max. from 0 to +70°C). Their use to produce the X-Detector, Y-Detector and, with gating, the Quadrant signals, is straightforward.

The remainder of the Detector Board logic is used for balance indication. Several of the operations involve balancing of the bridge and must be terminated when one or both of the synchronous detectors is nulled (within $\pm$1 step from zero). When the operation calls for nulling both detectors, the process continues clocking both X and Y registers until both detectors are cycling around zero.

The logic to properly indicate this balance condition is somewhat complicated because the detectors may be cycling in the same or in opposite directions with the transitions not precisely synchronous and with a possibility of comparator oscillations at the threshold. The method found best was to establish a time window when one detector reverses during which reversals of the other detector are counted. The clock rate is reduced after a certain number of counts and then, after additional counts, the process ends.

3.8 Detector Logic - continued

A positive transition of the X detector starts the time window by enabling the balance counter. Clock pulses are applied from the Y comparator to this counter. Logic is included to isolate the balance counter from possible comparator oscillations--the counter can be clocked only once per system clock cycle.

The duration of the window interval is established by the window counter which counts the system clock and thus adapts to changes in its rate.

One output of the balance counter controls the clock rate so that the balancing process proceeds rapidly until near the balance point. Additional balance counts are then required at the slow clock rate. Use of a two-speed clock significantly reduces the overall time required for a complete initial or final balance operation. The complete initial balance procedure requires about 3 seconds.

3.9 Servo Registers

The Autobalancing Unit requires a total of five Servo Registers which generate the $\emptyset$, X, Y, ΔX and ΔY control voltages and data. The digital portion of these boards is essentially identical and consists of three decade counters which drive a 12-bit digital-to-analog converter. The ΔX and ΔY Servo Register Boards also contain operational amplifiers to combine the coarse and fine analog outputs.

The digital circuits are straightforward and need no particular explanation. The decade counters may count up, count down, be reset, preset or disabled. All these functions are necessary. The D/A converters are relatively inexpensive yet are guaranteed both accurate and monotonic, over a 0-70^{o}C range. A full five-digit resolution is available from the combined X and ΔX and ΔY registers. This is possible only by

3.9 Servo Registers - continued

separation into coarse and fine 3-digit portions, with one digit overlap because a single D/A converter monotonic over this range is not available at any price. Monotonicity is absolutely necessary to avoid hangup of the servo system. The ΔY and ΔX Registers are preset to a half-scale value, the optimum setting of the interpolate registers during coarse balance.

Two cascaded op amps are used on the ΔY and ΔX Servo Register Boards, the first to sum the coarse, fine, and temperature compensation voltages, and the second to convert the output to a 0-25 V range. The circuits are conventional, but high quality components are required. Low offset voltage op amps are used and precision resistors are necessary to maintain accuracy. The ΔX circuit also has provision to sum an additional signal which is used to produce $\pm\Delta C$ offsets.

3.10 Command and Display Functions

The present Autobalancing Unit is intended primarily for semi-automatic operation. A manual command for one of the four basic operations is required to initiate a measurement sequence via a pushbutton switch on the front panel. The measurement then proceeds automatically. Completion of the required steps is indicated by a front panel light and the results are displayed on a digital readout. These data consist of 4 three-digit numbers corresponding to the X, ΔX, Y and ΔY registers.

The front panel controls are as follows:

CONTROL NAME	CONTROL TYPE	CONTROL FUNCTION
PWR	White alternate action illuminated pushbutton switch	Turns autobalancing units on/off
INT	Yellow momentary action illuminated pushbutton switch	Initial balance command. Latches on until another function selected.
FIN	Same as INT	Final balance command (w/o capacitive offset) Latches on until another function selected.
+ΔC	Same as INT	Final balance with positive capacitive offset command. Latching.
-ΔC	Same as INT	Final balance with negative capacitive offset command. Latching.
STOP	Red momentary action illuminated pushbutton switch	Indicates end of operation. Can be used to stop operation. Latching.
BRIDGE BALANCE DATA	3-digit numeric read-out	See text for units.
X/Y	Toggle switch	Selects X or Y balance data
COARSE/ FINE	Toggle switch	Selects coarse or fine balance data.
+ΔC	Grey knob	Sets positive capacitive offset
-ΔC	Grey knob	Sets negative capacitive offset
TEMPERATURE CONTROLLER COARSE	Screwdriver Adjustment	Sets coarse temperature
FINE	Screwdriver Adjustment	Sets fine temperature
GAIN	Screwdriver Adjustment	Sets servo gain of temperature controller

The balance data may be converted to give a value for the resistive or reactive bridge arm control voltage as follows:

$$V_{\substack{\text{Bridge}\\ \text{Control}}} = 25 \quad X \quad \left[\begin{matrix}\text{Coarse}\\ \text{Display}\\ \text{Value}\end{matrix} \quad 10^{-3} \quad + \quad \begin{matrix}\text{Fine}\\ \text{Display}\\ \text{Value}\end{matrix} \quad 10^{-5}\right] \text{volts}$$

The actual unknown being measured by the bridge can then be calculated using the varactor models, bridge equations, and correction factors.

Operation of the bridge temperature controller is described in a separate instruction book.

A number of connectors are located on the rear panel of the Autobalancing Unit, and are described as follows:

CONNECTOR NAME	CONNECTOR TYPE	CONNECTOR FUNCTION
AC LINE	Standard ac line male	110 V ac 60 Hz ac line power
OVEN FUSE	Standard fuse holder	Temperature controller power fuse
MAIN FUSE	Standard fuse holder	Autobalancing Unit power fuse
OVEN	MS female	Bridge temperature control oven interconnections (see Figure 3.10.1
X-DET	BNC Female	X-Detector signal from TSBD
Y-DET	BNC Female	Y-Detector signal from TSBD
PWR	5-contact Mini-hex female	DC power output (see Figure 3.10.2)
TSBD	7-contact Mini-hex female	Remove interconnections to TSBD (see Figure 3.10.3)
BRIDGE	9-contact Mini-hex female	Bridge interconnections (see Figure 3.10.4)
BUS	24-contact Blue Ribbon female	Remote data & control (see Figure 3.10.5)

Heater Cable

Bridge Connector (Amphenol Mini-Hex Type)	Wire Color ESMW-89-4			Autobal Connector
A	RED	}	HEATER	{ A
B	ORANGE			B
C	YELLOW	}	SENSOR 1	{ C
D	GREEN			D
E	BLACK	}	SENSOR 2	{ E
F	BROWN			F
H	SOLID BRIGHT and SHIELD	}	GROUND	G

Figure 3.10.1

POWER CABLES

A	RED	+15
B	BLUE	-15
D	GREEN	+ 5
E	BLACK	Gnd
H	NC	

Figure 3.10.2

TSBD Cable

Description: Multiconductor cable carrying Ø-programming and control signals between TSBD and Autobalancing Unit.

Connectors: Amphenol No. 126-195 7-pin miniature hexagon plug each end.

Cable: GenRad, Inc. ESMW-89-4, 7 #24 conductors (3 twisted pairs +1 single) shielded approximately 6' long.

Pin #:		
A	Ye-Wt	Ø Mode
B	Bn-Wt	Ø Volt
C	Gn-Wt	Timer
D	Bk-Wt	Gnd
E	Rd-Wt	Search
F	Or-Wt	Search
H	None	None

Figure 3.10.3

Bridge Cable

Description: Multiconductor cable carrying bridge control and temperature sensing signals between Microelectronic Bridge and Autobalancing Unit.

Connectors: Amphenol No. 126-220, 9-pin miniature hexagon plug each end.

Cable: (see TSBD cable)

Pin #	Wire Color and Pairs	Use
A	Bn-Wt	Temp sensor
B	Bk-Wt	Temp sensor gnd
C	Rd-Wt	R-voltage
D	Gn-Wt	R/C-voltage gnd
E	Or-Wt	C-voltage
F	None	None
H	None	gnd remote ø
J	None	gnd jumper
K	None	None

Figure 3.10.4

Autobalancing Unit

Data Output Connector

(mates with Amphenol #57-30240)

PIN #	SIGNAL		
1	1		
2	2		
3	4	LSD	BCD Data
4	8		positive true
5	10		"0"=Gnd "1" = +5V
6	20		CMOS output
7	40		Buffer with CMOS
8	80		device such as
9	100		CD4010 before
10	200		driving TTL load
11	400		
12	800		
13	X/Y		Word Select/
14	Coarse/Fine		Command
15	NC		(see below)
16	NC		
17	NC		
18	NC		
19	INT		Command Inputs
20	FIN		momentary contact closure
21	+ΔC		to gnd (by switch, relay,
22	-ΔC		or open-collector TTL device)
23	STOP		
24	Gnd		

Word Select/Command is an output indicating data word selected by front panel switches or, with switches in any position, can be used to externally command desired word:

Figure 3.10.5

3.11 Bus Interfacing

A calculator-based crystal measuring system using the standard IEEE interface bus was studied during this work on the Autobalancing Unit. Such a system would require two complete Talker-Listener bus interfaces, one for the Autobalancing Unit and one for the frequency synthesizer.

These bus interfaces can be thought of as two parts, one being the actual interconnection to the bus and the other being the special control logic necessary to control the operation of the particular unit under consideration. The former is a relatively standard design that need not be discussed here. The latter will be described in order to document the results of our study of these requirements.

3.12 Autobalancing Unit Control Interface

The Autobalancing Unit would require a complete Talker-Listener bus interface for use in a calculator-based system. It would have to receive, as a minimum, commands from the calculator to initiate the basic measurement sequences. This could be easily encoded by assigning one of the eight data lines to each command. It may also be desirable for the calculator to send data representing $\pm\Delta C$ offset information to the Autobalancing Unit. This would be applied as preset data to the X and ΔX registers. Provision for presetting all of the other registers would also be desirable.

The Autobalancing Unit would have to transmit balance voltage information to the calculator, the contents of the X, ΔX, Y and ΔY registers. These data

are now multiplexed into a single three-digit readout. Simple control logic can apply these data to the bus. The assertion of the first datum would signal the completion of the measurement.

3.13 Δf Counter

High resolution frequency data could be obtained for the system by a Δf counter which would accept an auxiliary Δf signal from the frequency synthesizer, count it, and place the resulting data on the interface bus. The Δf signal is available as a special modification from the GR 1061/1062 synthesizers. It varies from 5.0 to 5.1 MHz over the range of a selected digit and makes available expanded resolution frequency information. An X1000 resolution expansion, for example, permits 1 millihertz resolution by counting for one second. This represents a fractional frequency resolution of 1×10^{-10} at 10 MHz.

The counting circuits would be straightforward. TTL devices would be used in the input comparator and first decade at 5 MHz, and the remaining six decades could use CMOS devices. The output data would be multiplexed onto four lines with tri-state hex buffers organized into 4-bit sections.

The control logic would be arranged according to the requirements of the IEEE interface bus standard. A counter and decoder would divide the process into 8 intervals, one for counting and seven for digit transmission. A counting interval of 1 second could be timed from the 1-MHz reference available from the synthesizer.

A complete paper design was done for the Δf counter but it was not breadboarded or tested.

3.14 Synthesizer Frequency Programming

The second bus interface would be required to allow a calculator to set the coarse synthesizer frequency.

The GR 1061/1062 synthesizers are externally programmed through a 50-pin connector on the rear panel. Ten-digit frequency information may be applied using a negative true BCD code. The selection of the "search" mode for analog control of a certain decade is done by programming a "10" or "A" for the particular digit, which must be 1-MHz steps or smaller.

The interfacing hardware would consist primarily of CMOS latches and TTL open collector hex inverters. The synthesizer has internal 2 KΩ pullup resistors on the programming lines.

The control logic would consist primarily of a 10-state counter and decoder. The data transmission begins upon receipt of a "listen" signal which would remove a reset level from the state counter. Receipt of successive "Data Flag" signals would clock data into the corresponding latch, and a "Data Accepted" would be sent back to the calculator and used to advance the state counter.

3.15 Objectives and Results

The main objective of the present Autobalancing Unit was to prove the basic concepts, not to build the most efficient logic implementation. While subject to many minor changes, the design evolved along the lines originally planned. The basic principle of digital servo registers followed by D/A conversion for the

phase and bridge control signals seems sound. The various operations are performed by executing a fixed series of steps depending only on a knowledge of the polarity of the synchronous detector outputs from the Tracking Servo Bridge Detector.

Nevertheless, while the basic objectives for the Autobalancing Unit have been met, the design process is far from complete.

Problem areas do exist and will be discussed in some detail in the following report sections. Furthermore, additional capabilities are necessary for operation of a calculator-based system.

The most serious problem is that the unit fails to stop at balance condition under some circumstances. This occurs if the last fine balancing operation is unable to reach balance within its adjustment range. No problem was experienced while using a simulated bridge, but the system does not operate satisfactorily with the actual bridge at frequencies below about 10 MHz.

The problem is caused by the extreme change in bridge sensitivity. (The magnitude of the in-phase and quadrature unbalance signal components per unit of the corresponding varactor control voltage.) The capacitive arm sensitivity decreases while the resistive arm sensitivity increases at low frequencies. This results in the capacitive arm control voltage required to maintain balance in the presence of a crosserror to exceed the range of the fine balancing servo. The simulated bridge operated at very low C varactor voltage which resulted in greater C arm sensitivity and thus no problem was experienced.

This difficulty, once recognized, should present no long range problem. It will be necessary to incorporate control system logic that will make coarse

adjustments if the fine adjustment cannot reach balance.

Another problem is speed and accuracy limitations. These factors are discussed in the next section. The present system requires about 3 seconds to make an initial balance and some improvement should be possible. The accuracy seems to be limited primarily by noise considerations. It is important to bear in mind that a manual balance is far slower and represents a much narrower effective noise bandwidth. Tests with the actual bridge above 10 MHz gave very encouraging results, with a scatter equivalent to under 0.1 pF.

3.16 Speed and Accuracy Limitations

The Autobalancing Unit has definite speed and accuracy limits which were studied both on paper and by actual test.

The initial balance process consists of seven steps, four of which are balancing-type operations which are subject to definite speed limitations imposed by the system bandwidth. The system performs these four operations to a resolution of 10^{-3}. For a simple analog system to settle to 10^{-3} with a step input requires about 7 time constants. The time constant of the X and Y synchronous detectors is about 5 msec, so these operations would require a total of about 150 msec. Digital servos are actually used for reasons of system programmability and infinite holding time. They can simulate the behavior of an analog servo by varying the clock rate in proportion to the unbalance signal. This is difficult to do over the entire dynamic range. The present system uses a two-speed clock as the simplest approach to achieving reasonable speed. The slow clock rate is determined by the system bandwidth while the optimum fast clock rate depends on the output change required. The total settling time is minimized when the ratio of fast to slow clock rate is approximately $\sqrt{N}$ where N is the number of steps required.

This represents the tradeoff between fast slewing, overshoot and slow correction to final value. The present hardware requires a number of cycles around the balance point to terminate a balancing operation. This makes slewing at a fast clock rate less desirable than it otherwise would be, making it impossible to reach the speed that would otherwise be possible with a two-speed clock.

It may also be worthwhile to reconsider the successive approximation approach, by which the balance condition would be reached not by simple counting, but by a "binary search" process. This approach was ruled out in this hardware because of increased complexity, the choice of direct BCD coding and, most importantly, the fact that two interacting variables are involved. Ordinary successive approximation hardware (such as used in some A/D converters) proceeds inflexibly from most to least significant bit weighings. If the "analog input" changes during the conversion process, as it most certainly would if two interacting variables were involved, the balancing process would not work. In order to successfully apply the successive approximation approach to this system, the process would have to have the flexibility to "backtrack" as necessary.

The successive approximation process would require far fewer "steps" to achieve balance. The required setting time for a large step is longer, of course, but an overall advantage is still possible.

While some improvements in speed are believed possible, it seems clear that 50 msec is not attainable, especially in view of the additional factor of noise as discussed next. Furthermore, extreme initial

balance speed is not considered of fundamental importance to the overall system. A time of 1 second is a practical goal.

The present system has a resolution of 10^5, 0.25-mV steps of bridge control voltage with a full scale of 25 V. The readings show noticeable scatter so it is necessary to understand the reason for this scatter before any useful consideration can be given to increased resolution.

It appears that the scatter is not caused by any hardware defect in the present system, but is caused by fundamental noise limitations.

A series of tests were made to see how the scatter varied with various system parameters and, in all cases, the results were in agreement with this conclusion. Most experiments were made by allowing the last fine initial balancing process to run continuously while recording the output of the fine D/A converter. The RMS scatter: (1) varies inversely with the RF power level applied to the bridge; (2) varies inversely with the square root of the system bandwidth; (3) is independent of the IF gain (as long as it is high enough to overcome the noise of the servo comparators; and (4) varies inversely with the transfer ratio of the bridge. Furthermore, the amount of scatter is in excellent agreement with the noise level of the receiver. This scatter in the C varactor balance voltage was 0.5 mV RMS around a nominal bias of 6.5 volt at a power level of 0 dBm into the bridge at 100 MHz.

Additional filtering will be required to make measurements to 0.1 mV at sub-microwatt power level into the unknown. An averaging time of about 250 msec would be required to achieve 0.1 mV rms scatter on the C varactor at 5 MHz with a power level of 1 microwatt

into 50 ohms. While passive filters could be switched in, it might be better to use the calculator to average the data. Another possibility is to raise the power level during initial balance.

There are many fundamental and practical factors which all interact to set speed and resolution limits in a system of this sort. The final answers will come only with additional work, but it is apparent that the specified 50 msec speed is unrealistic and that 0.1 mV resolution will require significant averaging time at low drive level.

3.17 Phase Adjustment Accuracy

The present Autobalancing Unit was found to have a phase adjustment error of around 15°. While not of any serious consequence for the actual balance data, this is far poorer than can be done manually. It seems reasonable to expect an accuracy of around 1°. A phase error of 0.6° would give 1% response in the quadrature channel sensitivities.

Experiments were conducted to gain a better understanding of the phase adjustment error which exists in the present Autobalancing Unit. The problem is apparently caused by the lack of a fine balance step ahead of the phase adjustment procedure. It seems likely that the inclusion of such a fine balance step would greatly improve the phase adjustment accuracy.

It is possible that several iterations of the phase adjustment process are required to achieve 1° accuracy (the manual process is also an iterative one). One can imagine an automatic process which iterates until a certain accuracy has been obtained.

3.18 Programmable Control Logic

The present autobalancing control system uses ordinary hard-wired logic. This approach was taken as the most straightforward, but, in retrospect, was probably unwise. It is now apparent that a system of this sort would benefit greatly from the use of programmable control logic. While ordinary hardware would still be used for D/A conversion registers and the analog circuits, the logic representing the steps in the balancing process would be replaced with software. Changes, such as iterative phase adjustment or alternative balancing procedures could be more easily tried and optimized. Even after the final control steps were decided upon, there would be the advantage of more effective operation. Total hardware complexity would be reduced, particularly for a system into which external data were to be loaded.

Serious consideration must be given to this approach in any future work.

3.19 Hardware Changes for Next Iteration

The present Autobalancing Unit hardware was used during the design process and, as such, was subject to many changes along the way. The main objective was to prove the concept, not build the most efficient logic implementation. It may, therefore, be useful to list some of the changes that would seem desirable for any future hardware.

1. The most efficient way to multiplex the output data from the X, Y, ΔX, and ΔY registers would be with tri-state CMOS inverting buffers.

2. The multiplex method above would take no extra hardware if the registers drove the D/A converters

directly as well as the output buffers. The complement data out of the registers and into the D/A converters would be inverted by the output buffers. The count up/down of the registers would effectively be reversed.

3. Only one state register/counter is required for both initial and final balance procedures. The entire control logic could then be consolidated into one section. The initial balance procedure could begin when the state register was reset and the final balance procedure when it was preset to a certain state.

3.20 Conclusions and Recommendations

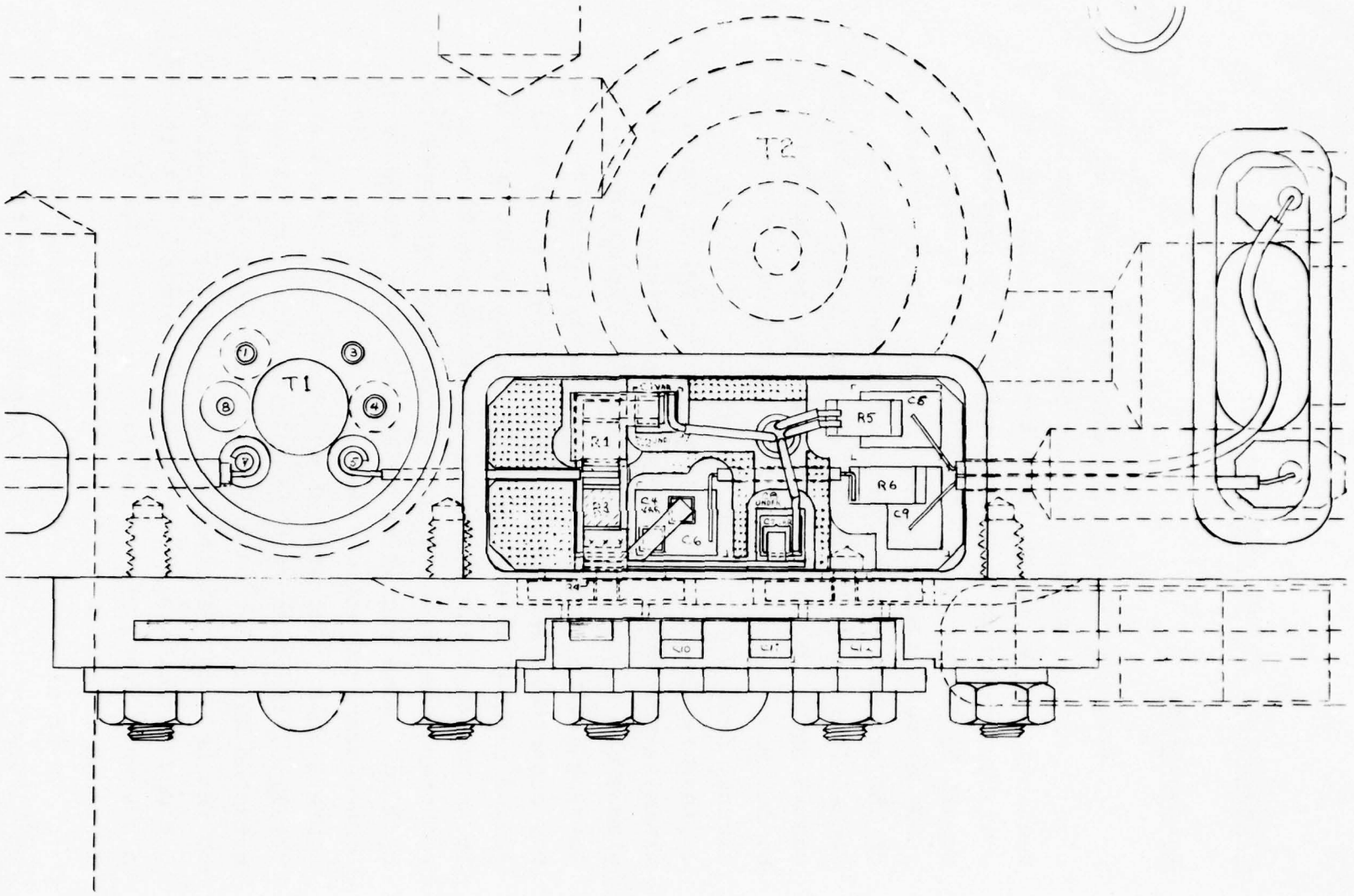
The present Autobalancing Unit hardware serves not so much to give final answers as to provide guidance on the best design and techniques that can ultimately lead to a satisfactory overall crystal measuring system. To follow all problems to their solutions was beyond the scope of the present contract. There was little time available to evaluate the Autobalancing Unit with the actual bridge.

4. MICROCIRCUIT BRIDGE ASSEMBLY

4.1 Introduction

A firm outline of the basic concept of a microcircuit bridge was provided by ERADCOM based on their continuing development of devices for measuring the characteristics of quartz resonators. A previous report by GenRad, part of ECOM-75-1341-F, was a paper study of such a microcircuit bridge. This section of the present report covers experimental work at GenRad including the design and assembly of an experimental model in a form that would be manufacturable by our Microelectronic facility. The use of a microcircuit device permits its placement in close, well-defined relationship to the resonator being tested to minimize connection errors and corrections, but this places the same severe environmental conditions on the testing device as imposed on the device under test. Our experience indicates that this requirement will demand careful attention to all construction details to insure that the microcircuit assembly will reliably withstand the repeated stresses induced by temperature cycling. Some sacrifice in electrical performance may be necessary to allow a mechanical design which will achieve this. Our present model consists of a mostly metallic structure with ceramic terminal insulators attached by solder as are all the individual components of the bridge. Figure 4.1.1 is a drawing approximately 5 times actual scale of the active portion of this model. A somewhat simplified schematic of the bridge circuit is shown in Figure 4.2.1.

In an effort to reduce parasitic inductance, particularly in the connection between the bridge



BRIDGE LAYOUT

Figure 4.1.1

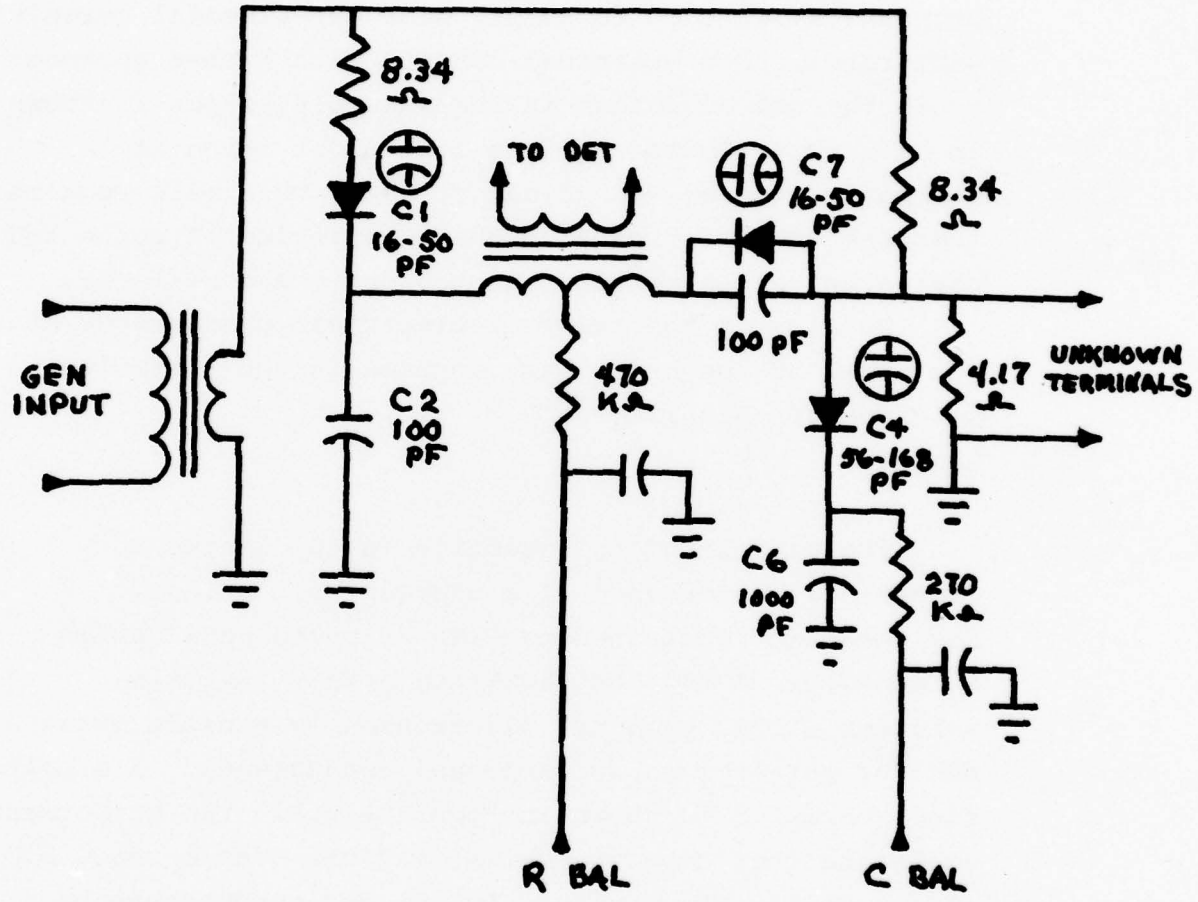


FIGURE 4.2.1

SIMPLIFIED SCHEMATIC MICROCIRCUIT BRIDGE

elements and the resonator under test, ERADCOM has proposed that a ceramic plate carry all the critical components as well as the terminals. This ceramic plate is then to be attached to a metallic structure to provide the necessary electrical isolation and ground returns, as well as a thermal connection to the assembly. GenRad has done no work on the later proposal other than to supply some experimental ceramic substrates. Our principal concern with either approach is in the use of solder in the assembly, which is known to have very limited fatigue life under repeated thermally induced mechanical stress. This will require that the thermal expansion characteristics of connected pieces be very carefully matched or stress relieved.

Details of the study of electrical performance of our model of the bridge are covered in the following sections of this report.

4.2 General

The purpose of this section is to discuss the electrical performance of a microcircuit bridge, designed and fabricated by GenRad, based on a design by ERADCOM. A modified Schering bridge utilizing varactor diodes provides electronically tunable measurement of parallel capacitance and conductance. A simplified schematic is shown in Figure 4.2.1. The performance goals are that capacitance be read out over a range of +20 pF to -20 pF to within 0.1 pF and conductance be read out as parallel resistance over the range of 2 ohms to 20,000 ohms to within 5%. How well our model met these goals is discussed in the following sections.

The thrust of our effort was to provide affirmative answers to the following questions:

1. Can the capacitance versus voltage of varactor diodes be characterized over the required temperature range (-50 to 105°C) so that the readout in terms of the desired parameters be obtained by computation from the applied voltages?
2. Can the effect of the conductance-varactor diode-control-voltage feed circuit on the "C" balance at low frequencies be minimized or eliminated?
3. Can the bridge transformer be improved to minimize its contribution to measurement errors?
4. Can the overall assembly be arranged so that it is practical to hermetically seal it to eliminate detrimental effect of atmospheric moisture on leakage resistance of the varactors?
5. Can parasitic impedances be reduced by careful design so that acceptable accuracy can be achieved directly or with a reasonable number of corrections by means of a desk-top calculator/controller?

4.3 Varactor Diodes

The usual mathematical expression used for the capacitance of varactor diodes is as follows:

$$C_T = \frac{C_{OV}}{\left[1 + V_{R/\phi}\right]^r} + K$$

where C_T = Terminal capacitance of device

C_{OV} = Junction capacitance at zero reverse voltage

ϕ = Diode contact potential ($\approx$ 0.6 for silicon)

r = Diode power law ($\approx$ 0.44 for abrupt junctions)

K = A constant (fixed C in shunt with junction)

V_R = Applied reverse voltage

We find that if C_{OV}, ϕ, r and K are empirically adjusted, we can obtain excellent agreement between the mathematical

value of C_T and the measured capacitance of any particular diode with applied reverse voltages of one volt or more. With any value of K a three point match can be obtained by adjusting C_{OV}, Ø, and r. Choosing match points at 1, 4 and 20 volts has been found to consistently yield symmetrical peak capacitance errors at intermediate voltages. The error curve has a characteristic horizontal "S" shape with the error reversing between successive match points. If the magnitude of the error is unacceptable, the constant, K, can be adjusted to reduce it (of course, other constants must also be changed to preserve the 3 point match.) For example, Figure 4.3.1 is the error curve for a particular varactor using K = 0. Figure 4.3.2 is the error curve for same varactor with $K = -5 \times 10^{-12}$, which shows a significant and symmetrical reduction in the deviations in C from that of the mathematical expression. Figures 4.3.2 and 4.3.3 are the error curves for the varactors C1 and C4, respectively, used in the bridge fabricated by GenRad. Since the varactors are exposed to the full temperature range of the measuring system, a temperature compensation scheme is needed to retain the readout accuracy required. Two methods are considered to be equally satisfactory:

1. Replace V_R in the expression for C_T by $V_R - Q(T-25)$ and supply the constant Q and the variable T for the mathematical calculation, where T is the temperature of the bridge obtained from the controller or accurate temperature sensor.

2. Provide a totally analog correction to the voltage applied to the varactor by summing a portion of the voltage drop across two forward biased silicon diodes, mounted to sense the bridge temperature, with the control voltages applied to the varactors.

The second method seems easier to implement unless accurate bridge temperature is already available in digital form for the calculator. Figure 4.3.4 is the

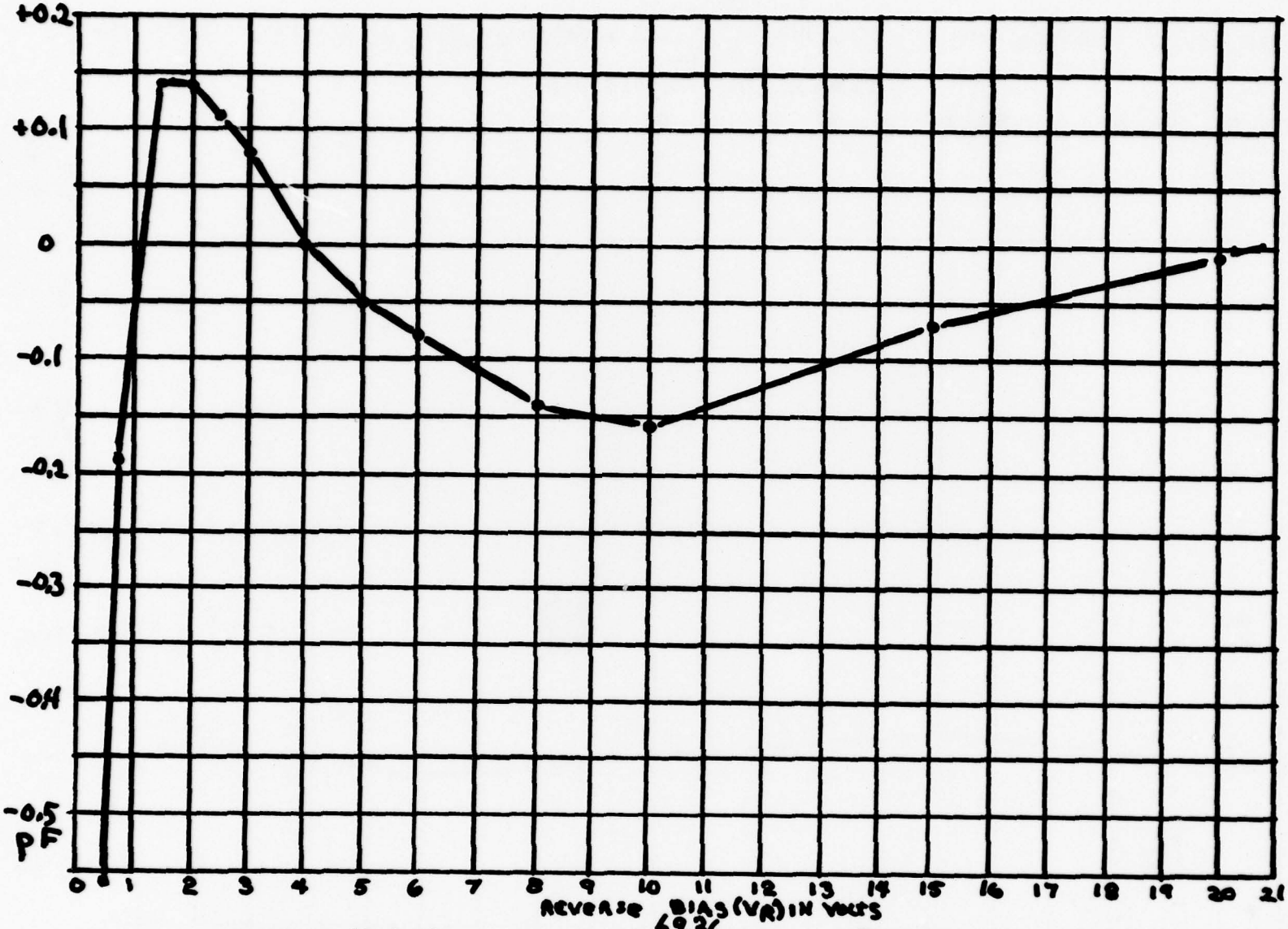


FIGURE 4.3.1 DEVIATION OF C_T (CALCULATED) $= \frac{69.36}{\left[1+\frac{V_R}{1.03}\right].485}$ pF FROM MEASURED VALUES OF C1

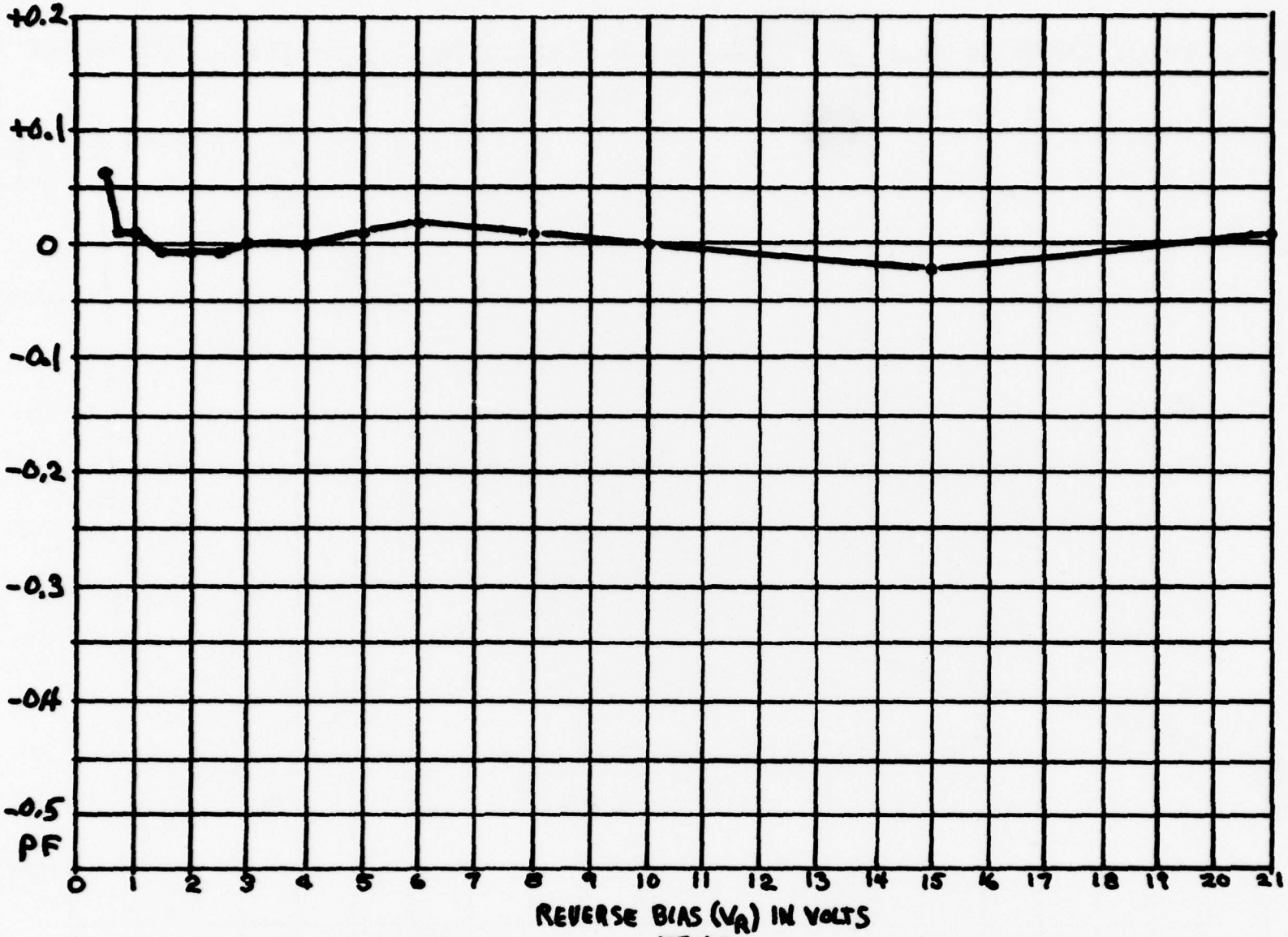


FIGURE 4.3.2 DEVIATION OF C_T(CALCULATED) $= \frac{77.64}{\left[1+\frac{V_R}{.675}\right]^{.381}} - 5$, pF FROM MEASURED VALUES OF C1

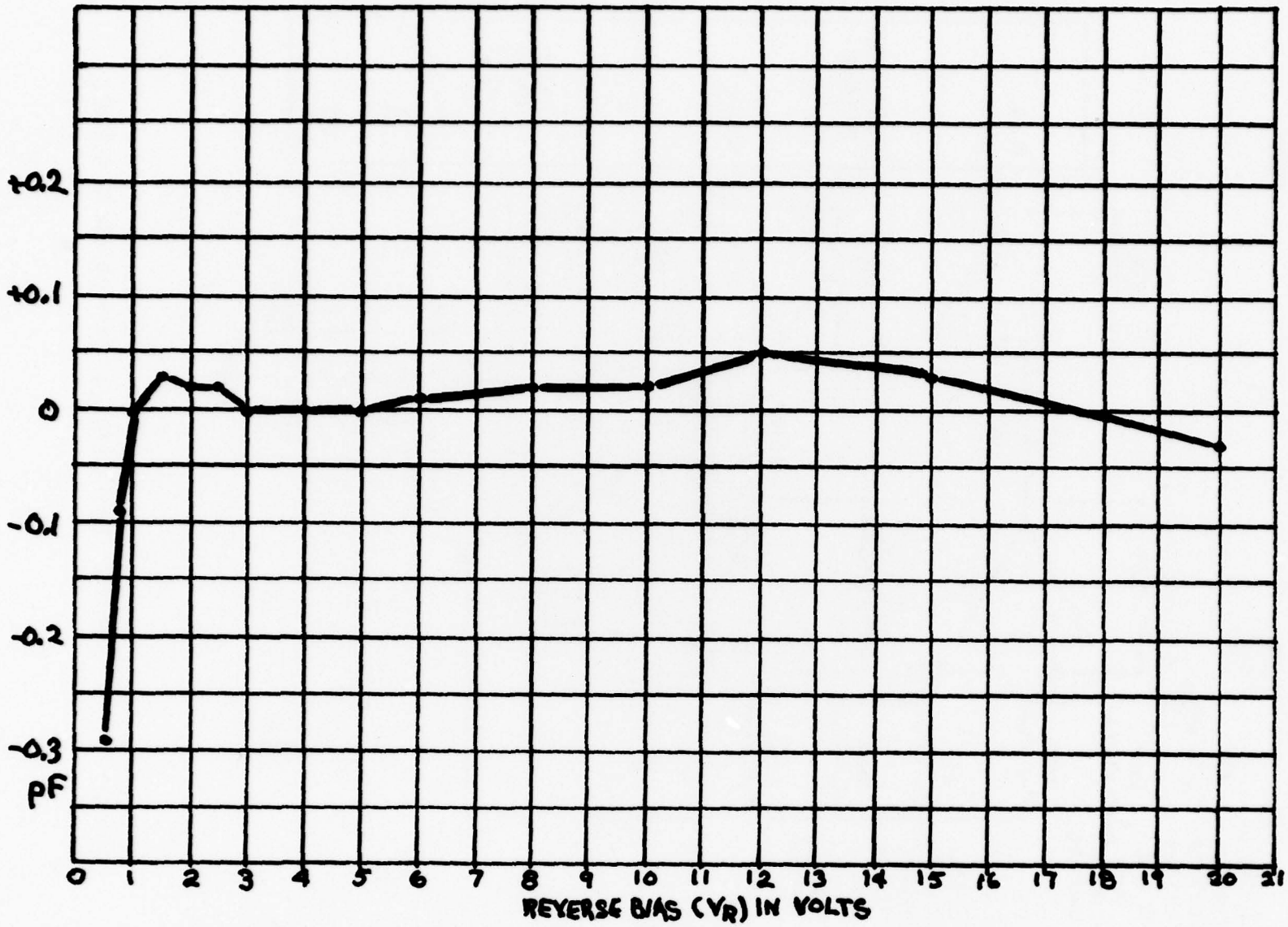


FIGURE 4.3.8 DEVIATION OF C_T(CALCULATED) $= \frac{255.76}{\left[1+\frac{V_R}{.778}\right]^{.48}} + 3$, pF FROM MEASURED VALUES OF C4

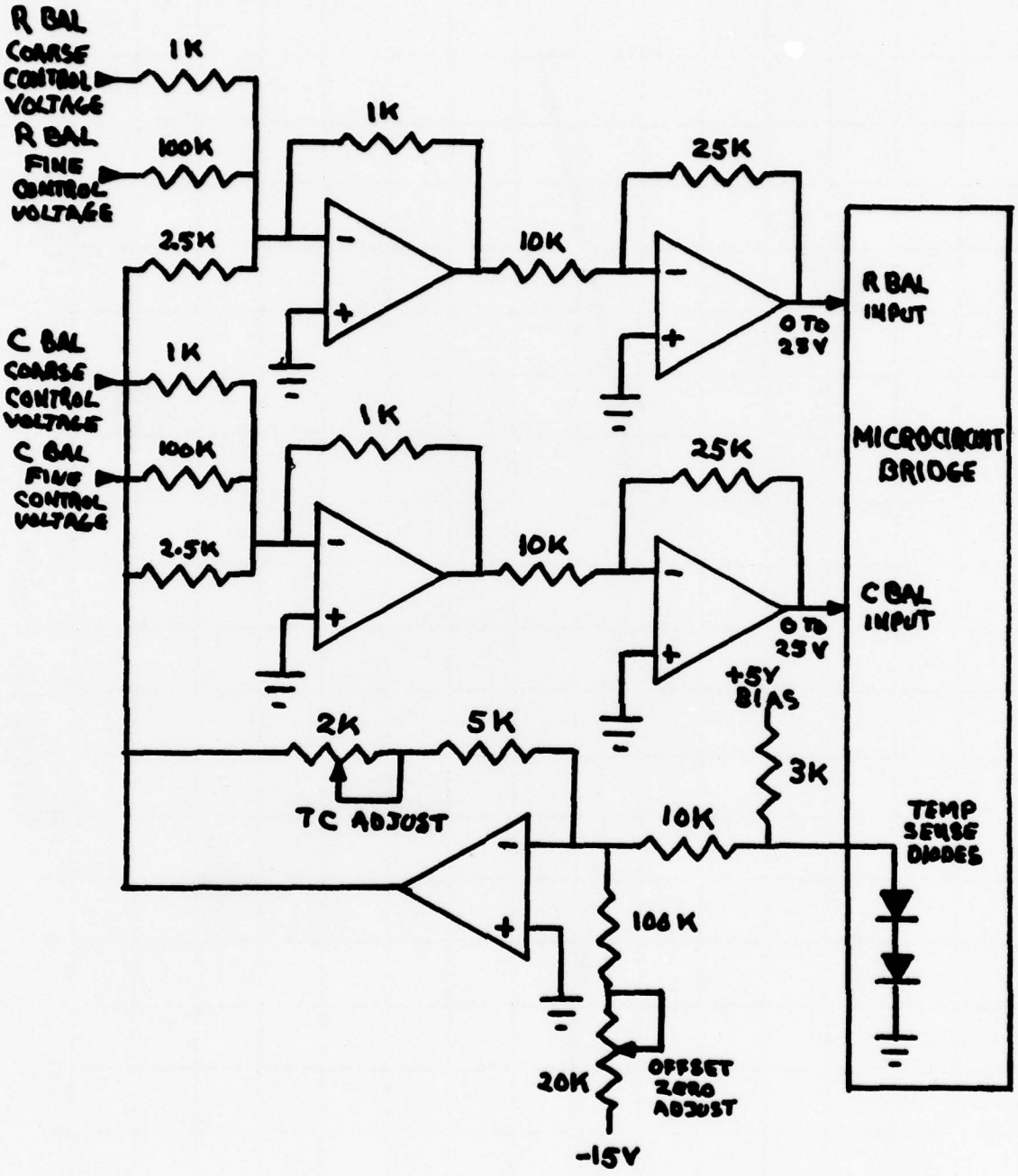


FIGURE 4.3.4 ANALOG TEMPERATURE COMPENSATION CIRCUIT

schematic of the analog temperature correction scheme used in the GenRad model of the bridge.

4.4 Conductance Balancing Varactor Feed Compensation

An RC filter is required to feed the dc control voltage to the conductance balancing varactor while providing an RF signal path to the detector transformer. For any practical values of R and C, this produces a small but significant phase shift at the low end of the frequency range which must be compensated by the C balance. An inherent characteristic of the bridge is a constant delta C range at the unknown terminals, but this represents a diminishing phase shift as the operating frequency decreases. The available correction for any initial balance bridge phase errors is therefore extremely limited at the low frequency end of its range. In addition, when measuring a conductive device the amount of phase correction is altered, resulting in a significant cross term in the readout of C_p due to R_p.

The latest ERADCOM models use a small value fixed coupling capacitor at the "unknown" side of the detector transformer and feed the dc control with a high value resistor to the transformer primary center tap. This improves the situation for initial balance in that when the value of the coupling capacitor is properly chosen, the same phase shift occurs at each end of the detector-transformer primary and no compensating offset is required by the C balancing varactor. However, when an "unknown" resistance is connected, the conductance balancing varactor must be changed and a cross term appears. The GenRad model compensates for this by placing a tracking varactor, C7, across the coupling capacitor which maintains symmetry of source impedances for the detector transformer and phase compensation for

all settings of the conductance balance. See Figure 4.2.1 for circuit details.

4.5 Detector Transformer

The full voltage applied to the "unknown" appears at each end of the primary winding of the detector transformer, even when the output voltage is nulled for bridge balance. Any common-mode coupling will appear in the output and tend to obscure the balance. The latest ERADCOM experimental bridges that we examined used cascaded RELCOM-type subminiature transformers, two standard 200/50-ohm types and one modified with a special double-balanced winding. These transformers have no inter-winding shields and depend entirely on center-tap-grounded windings to balance out lateral capacitive coupling between windings. Figure 4.5.1 is a schematic of this arrangement. Figure 4.5.2 shows the performance of this transformer system assembled by GenRad measured as insertion loss with a 50-ohm source and load. For the common-mode measurement the two ends of the input winding are tied together (center tap floating) and the source applied between this point and ground. The source impedance in the actual bridge circuit consists of a 100- to 150-pF capacitor in each input lead which produces low-frequency roll-off for the normal mode and influences the effective common-mode coupling. For example, a transformer showing extremely low common-mode coupling, as measured as described above, can have very high effective common-mode coupling if the series source capacitors as well as the stray capacitance from each input terminal to ground are not perfectly matched. Any unsymmetrical capacitance introduces currents into the input winding which are coupled by the normal mode to the output. Of

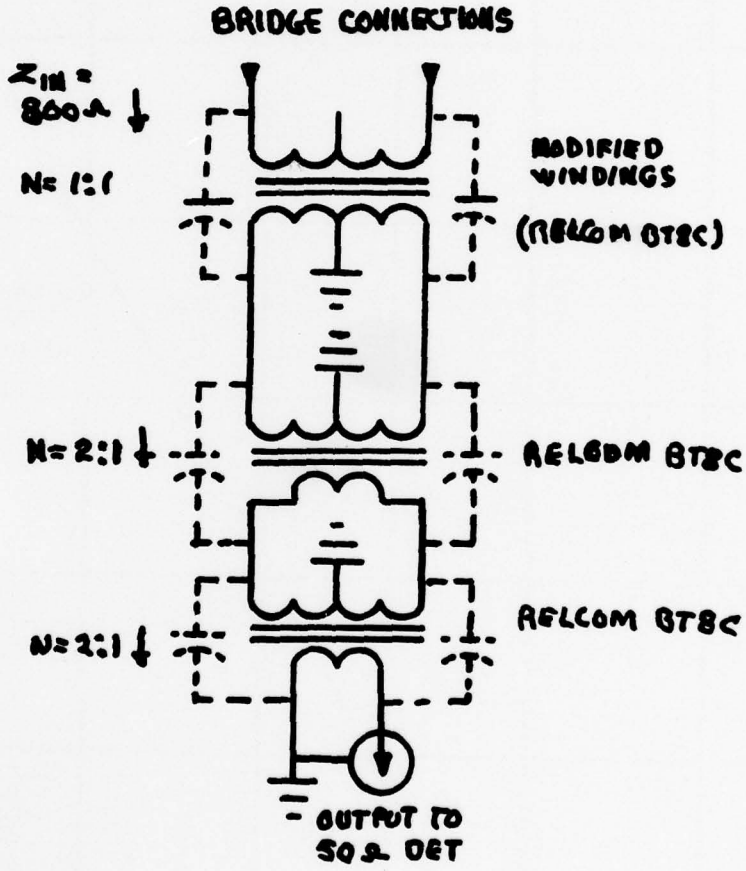


FIGURE 4.5.1

ERADCOM DETECTOR TRANSFORMER SCHEMATIC

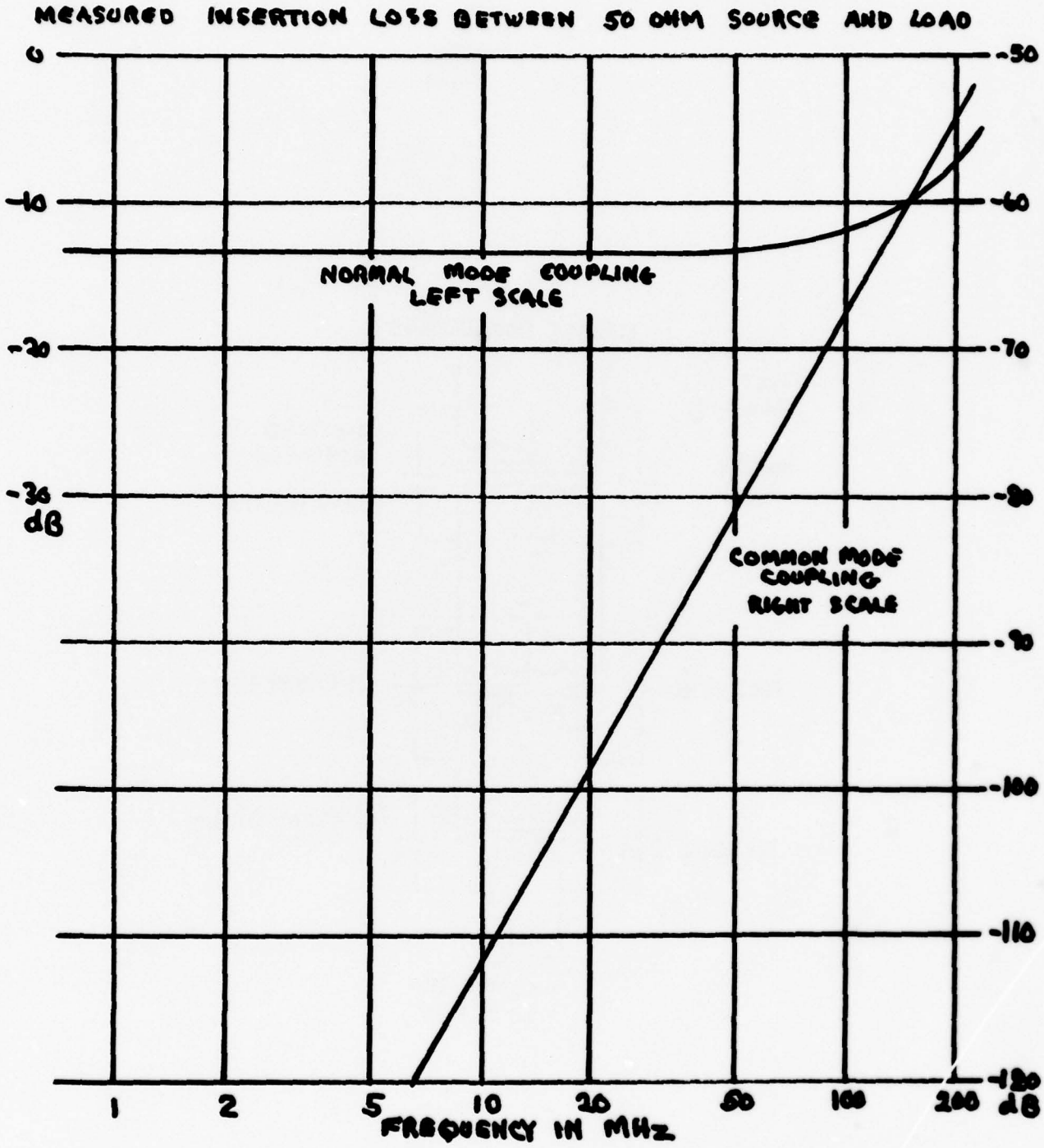


FIGURE 4.5.2 PERFORMANCE OF ERADCOM DETECTOR TRANSFORMER

course, if the stray capacitances are negligible compared to the source capacitances, the effect of any unbalanced capacitances are negligible but this is not the case for any practical transformers for this bridge. For our modified RELCOM transformer we measure a total primary to ground capacitance of 14 pF which is no doubt due to the close proximity of primary and secondary windings. With better wire insulation and/or lighter twisting, or perhaps parallel windings, much lower capacitance is possible. Any added leads at the primary, particularly the coaxial shielded leads used in some experimental models of the bridge, add to the capacitance and increase the possibility of unbalanced capacitance to ground.

In our model of the bridge we attempted to minimize the capacitance to ground by designing a transformer with a heavily insulated primary, arranged in the assembly to connect to the required points in the bridge with minimum-length symmetrical self-leads. Figure 4.5.3 is a schematic of this transformer. It has an electrostatically shielded secondary to minimize common-mode coupling due to capacitance between windings. The primary consists of a twisted pair of wires in teflon tubing to isolate it from the grounded-secondary shield and transformer core. Measured total primary to ground capacitance is 5 pF. Figure 4.5.4 shows normal and common-mode couplings measured by the method described for the RELCOM transformer system except in this case the transformer was in the actual bridge assembly utilizing the shielding and terminal connections thereby provided. It should again be noted that the performance in the final bridge configuration is modified by the effective series source capacitances presented by the bridge circuit which produce a low-frequency roll off of the normal mode coupling and influence the effective common-mode coupling. Since the capacitance to ground has been reduced by almost a factor of 3 over our RELCOM

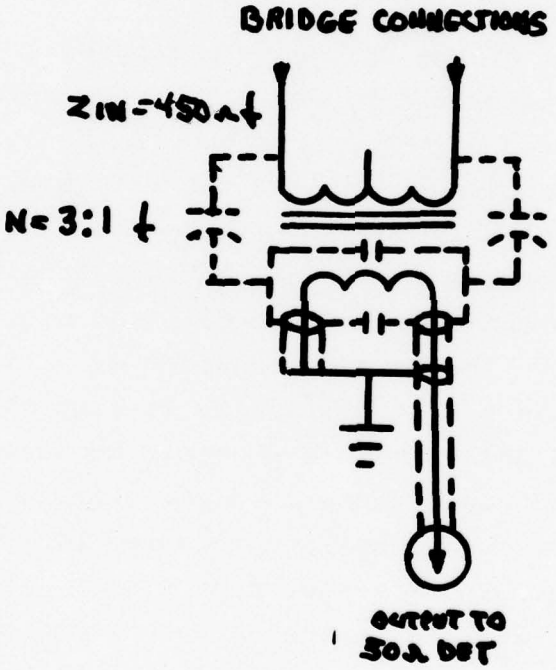


FIGURE 4.5.3

GENRAD DETECTOR TRANSFORMER SCHEMATIC

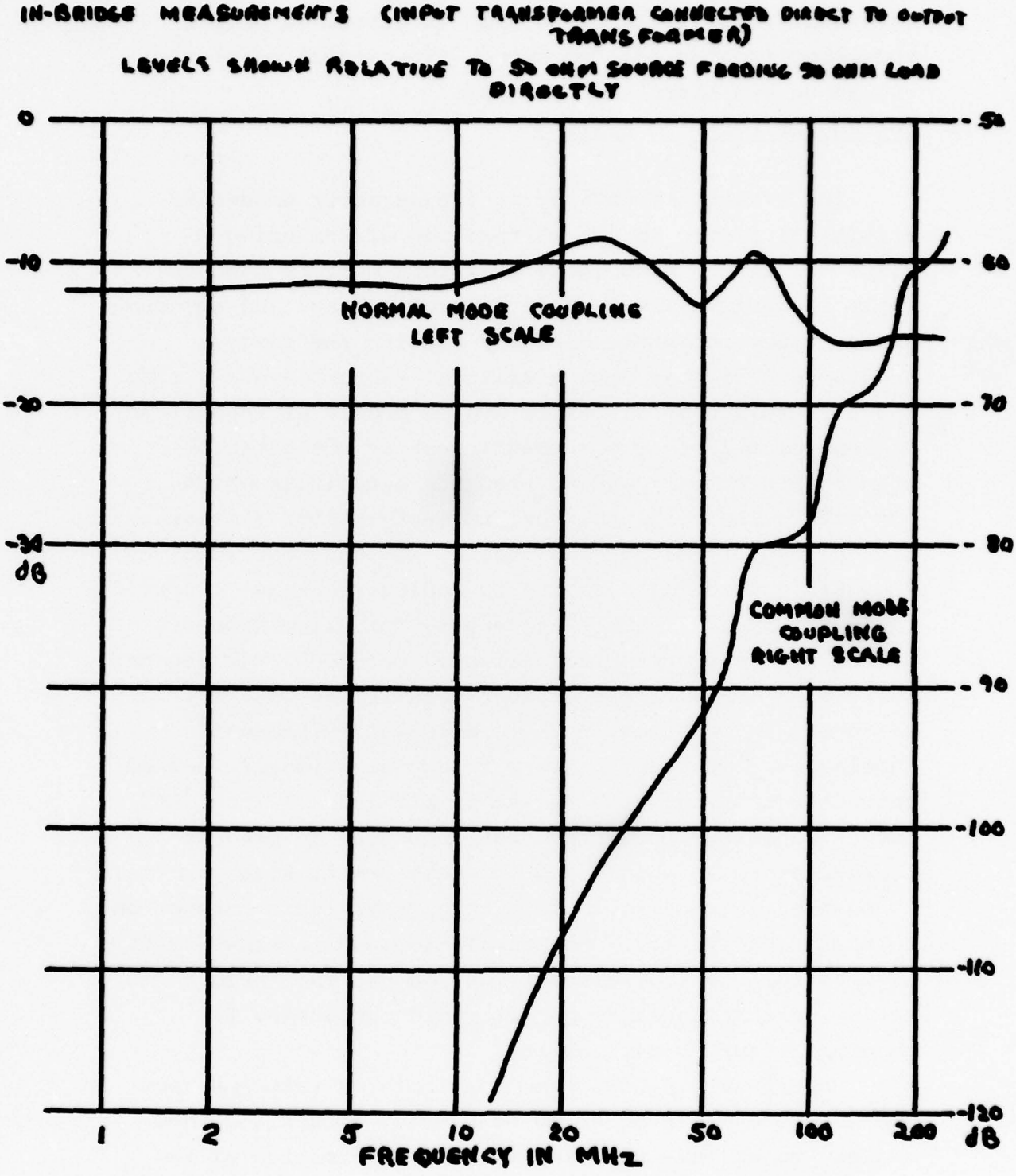


FIGURE 4.54. PERFORMANCE OF GENRAD DETECTOR TRANSFORMER

arrangement, a similar reduction in effective common-mode coupling for a given source capacitance unbalance should be exhibited in actual use.

4.6 Design for Hermetic Sealing

The leakage resistance of the varactor diodes is a critical factor in the performance of the bridge since relatively high value resistors must be used to apply the externally applied control voltage and any drop across these resistors directly affects the readout accuracy. This has been a critical factor in evaluating the performance of all experimental models of the bridge. Of course, all other components such as the detector transformer primary and dc blocking capacitors which connect to the diode feed points must exhibit similar high values of leakage resistance. It has been long recognized that the best way to achieve this is to provide a completely dry, stable atmosphere for all components of the bridge by hermetic sealing. Our model was designed to provide means of evacuating, backfilling with dry nitrogen, and sealing, using a cold-weld-pinch-off tubulation. Special adaptors to SMA hermetically sealed connector bushings from the semirigid coaxial input and output cables to the bridge were designed to prevent leakage at these points and the measurement high terminal is mounted on a ceramic plate which seals this connection to the bridge cavity. The tubulation and internal ports between the transformer cavities and the main bridge cavity were designed to permit rapid outgassing the assembly prior to backfilling.

Unfortunately, the time available on this contract did not permit our model to be pumped, backfilled, and sealed, so we have no experimental verification of the success of this part of the design. A rapid deterioration of the performance of our unsealed model has occurred

since it left the confines of our air-conditioned laboratory, and this could be due to the absence of such protection.

4.7 Measured Performance of Our Model

4.7.1 Resistance Initial Balance

Figure 4.7.1 shows the variation of capacitance value of the resistance balancing varactor versus frequency as inferred from the applied dc voltage using the relationship given in Figure 4.3.2.

4.7.2 Capacitance Initial Balance

Figure 4.7.2 shows the variation of capacitance value of the capacitance balancing varactor versus frequency at various RF levels as inferred from the applied dc voltage using the relationship given in Figure 4.3.3.

4.7.3 Bridge Orthogonality at Initial Balance

Figure 4.7.3 shows bridge orthogonality between C and R initial balance adjustments versus frequency measured by observing the change in reference phase to quadrature phase-sensitive detectors required to eliminate C detector output due to R balance offsets relative to phase setting for the reverse situation.

4.7.4 Measured Values of Thick-Film Resistors

Figures 4.7.4.1, 4.7.4.2, and 4.7.4.3 are plots versus frequency of measured values of effective series resistance and inductance of thick-film resistors of 5 to 1,000 ohms nominal dc values. Measured values shown include corrections for the effect of 0.9 nH series inductance in C2, 0.71 nH series inductance in C6, and 2.08 nH series inductance in the "unknown" terminals of the circuit shown in Figure 4.2.1.

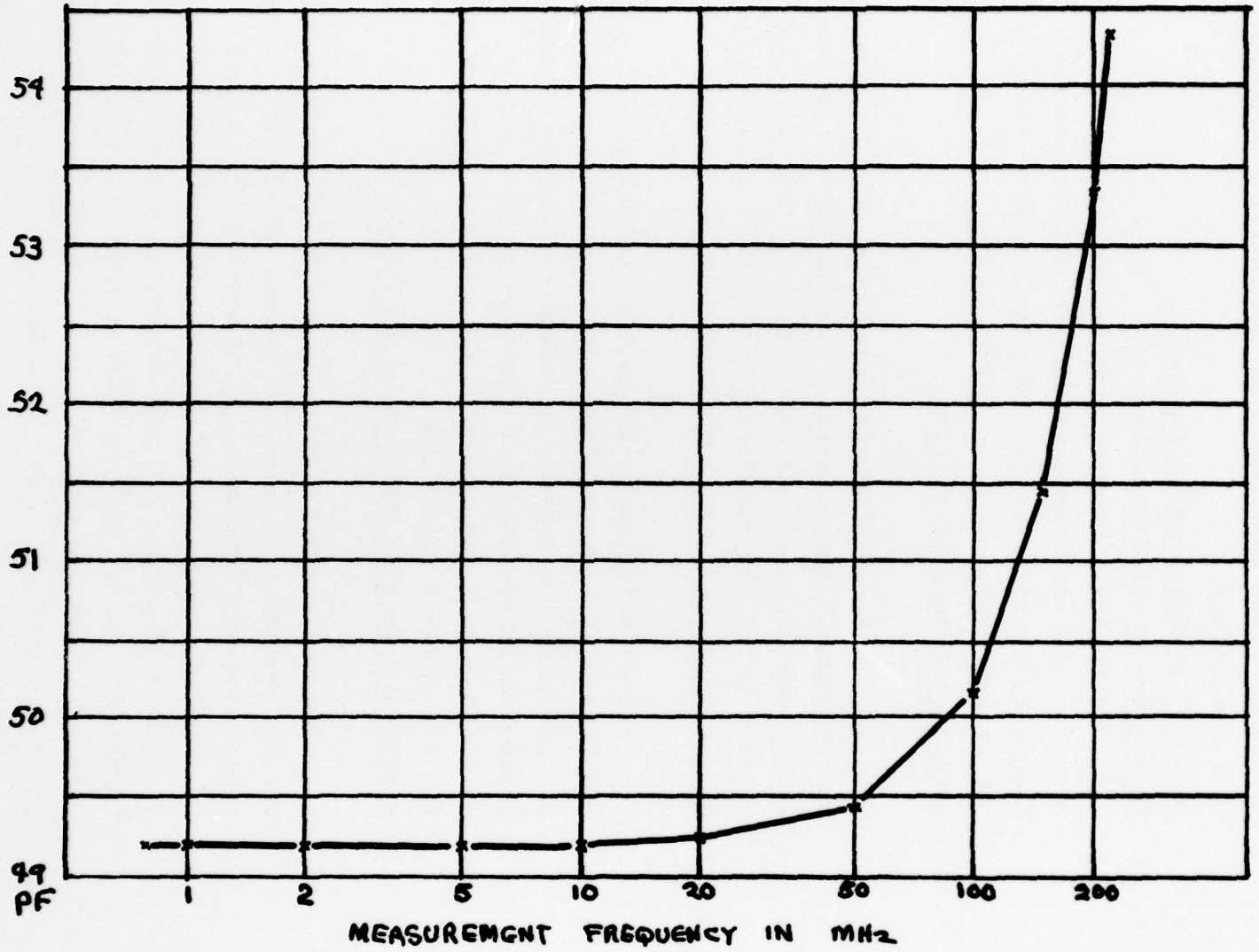


FIGURE 4.7.1 RESISTANCE INITIAL BALANCE CAPACITANCE, C_{10}

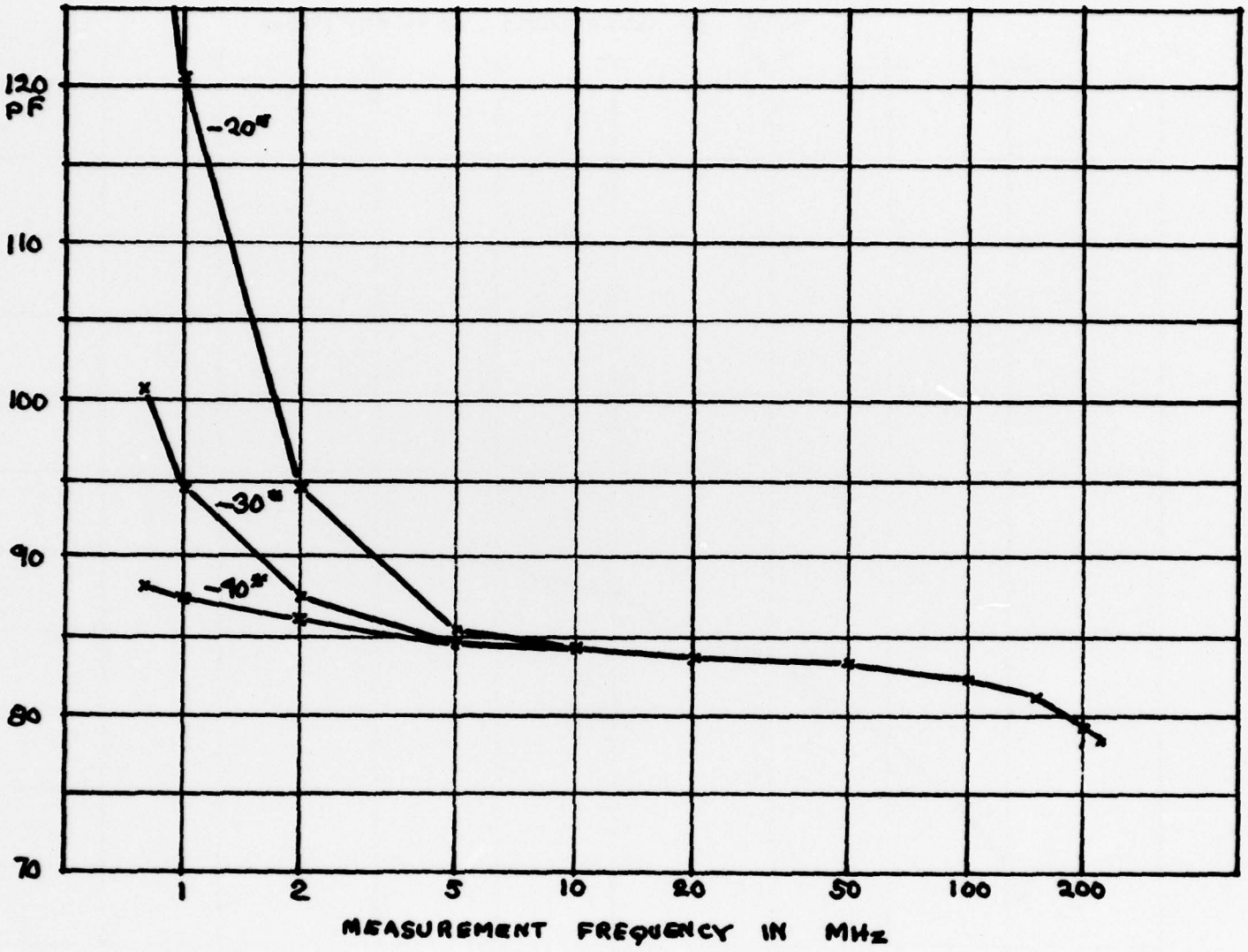


FIGURE 4.7.2 CAPACITANCE INITIAL BALANCE, C_{40}

* RF LEVEL ATTENUATOR SETTING ON T.S.B.O.

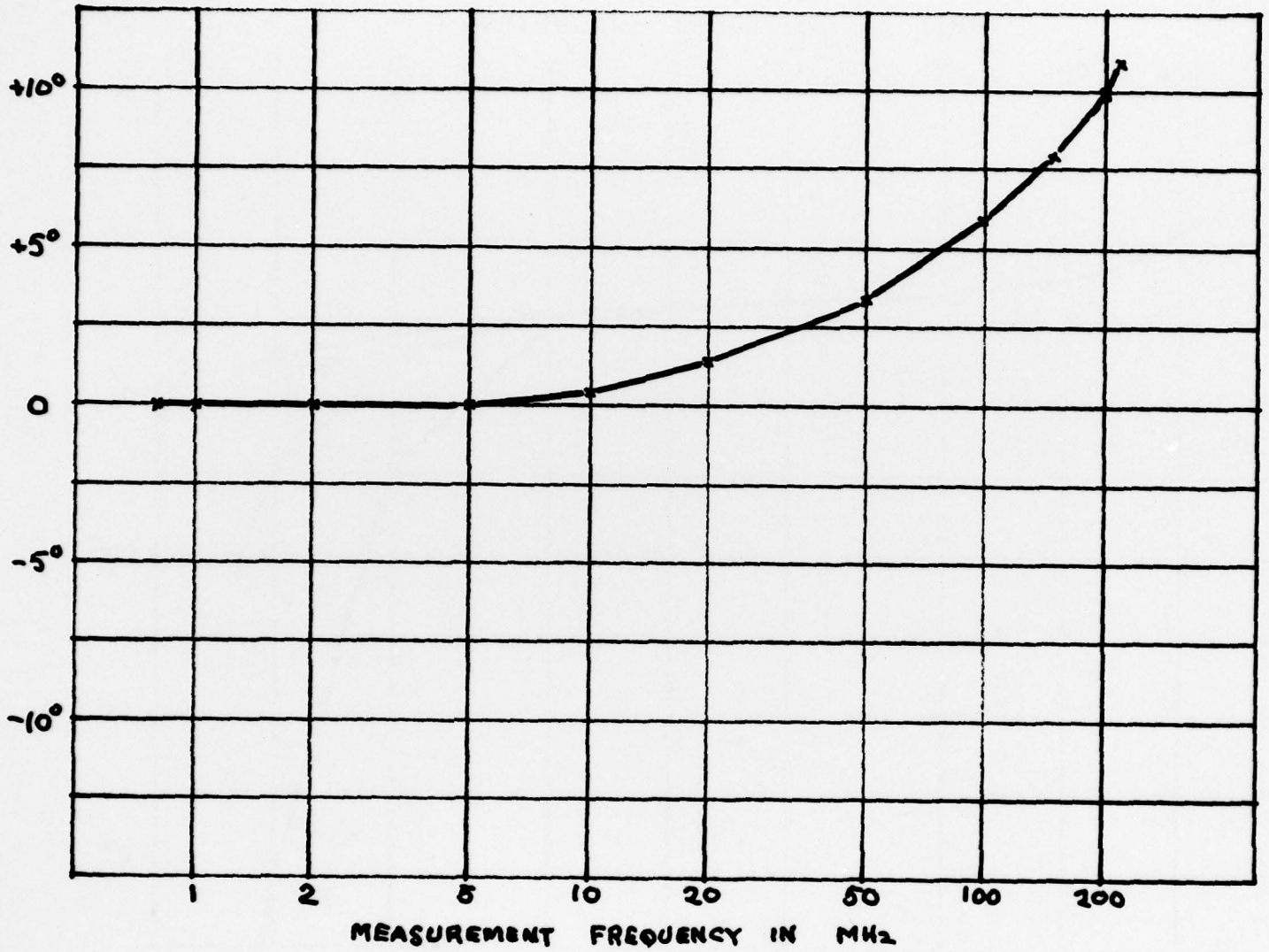


FIGURE 4.7.3 BRIDGE ORTHOGONALITY AT INITIAL BALANCE

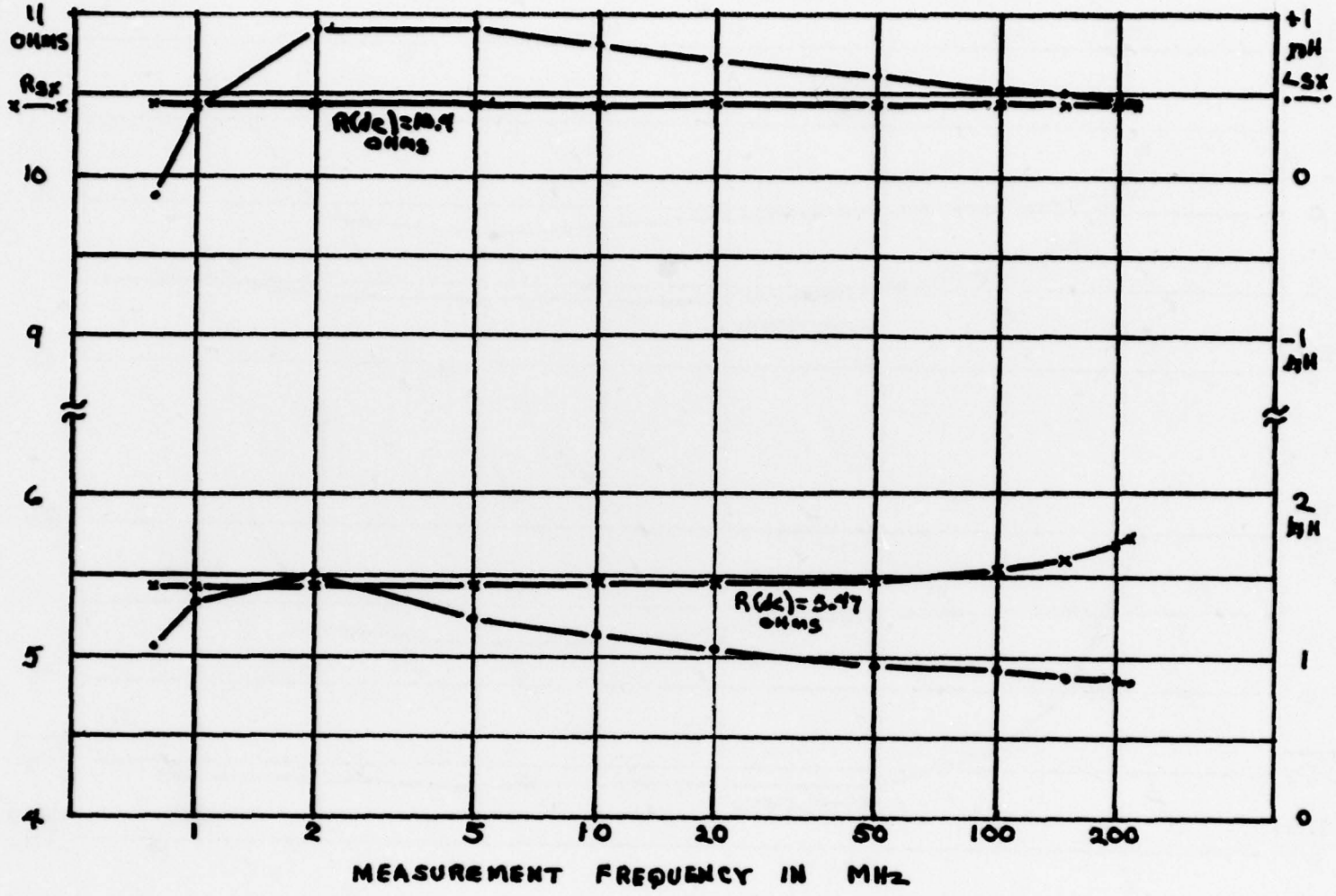


FIGURE 4.7.4.1 MEASURED VALUES OF THICK FILM RESISTORS

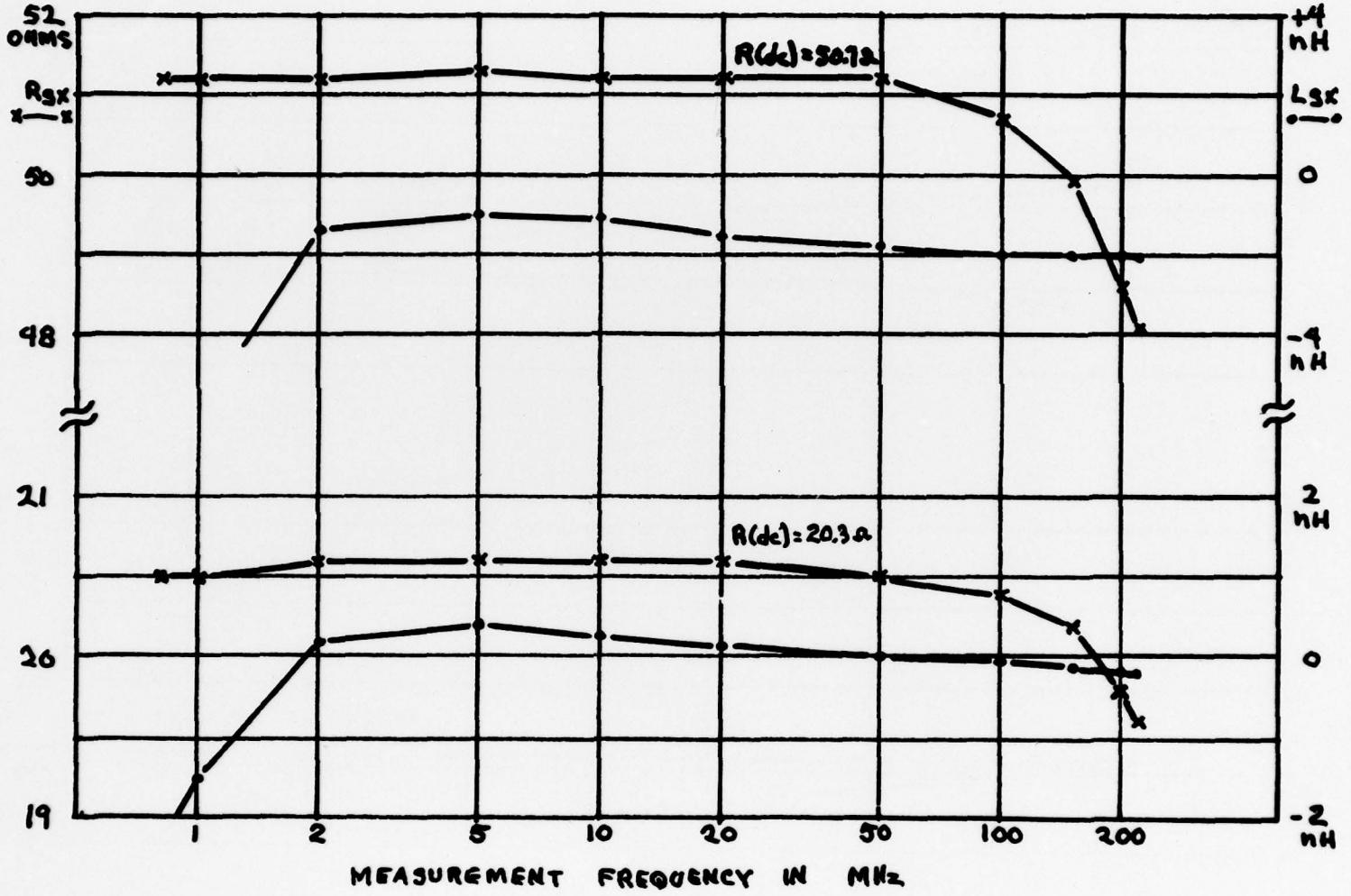


FIGURE 4.7.4.2 MEASURED VALUES OF THICK FILM RESISTORS

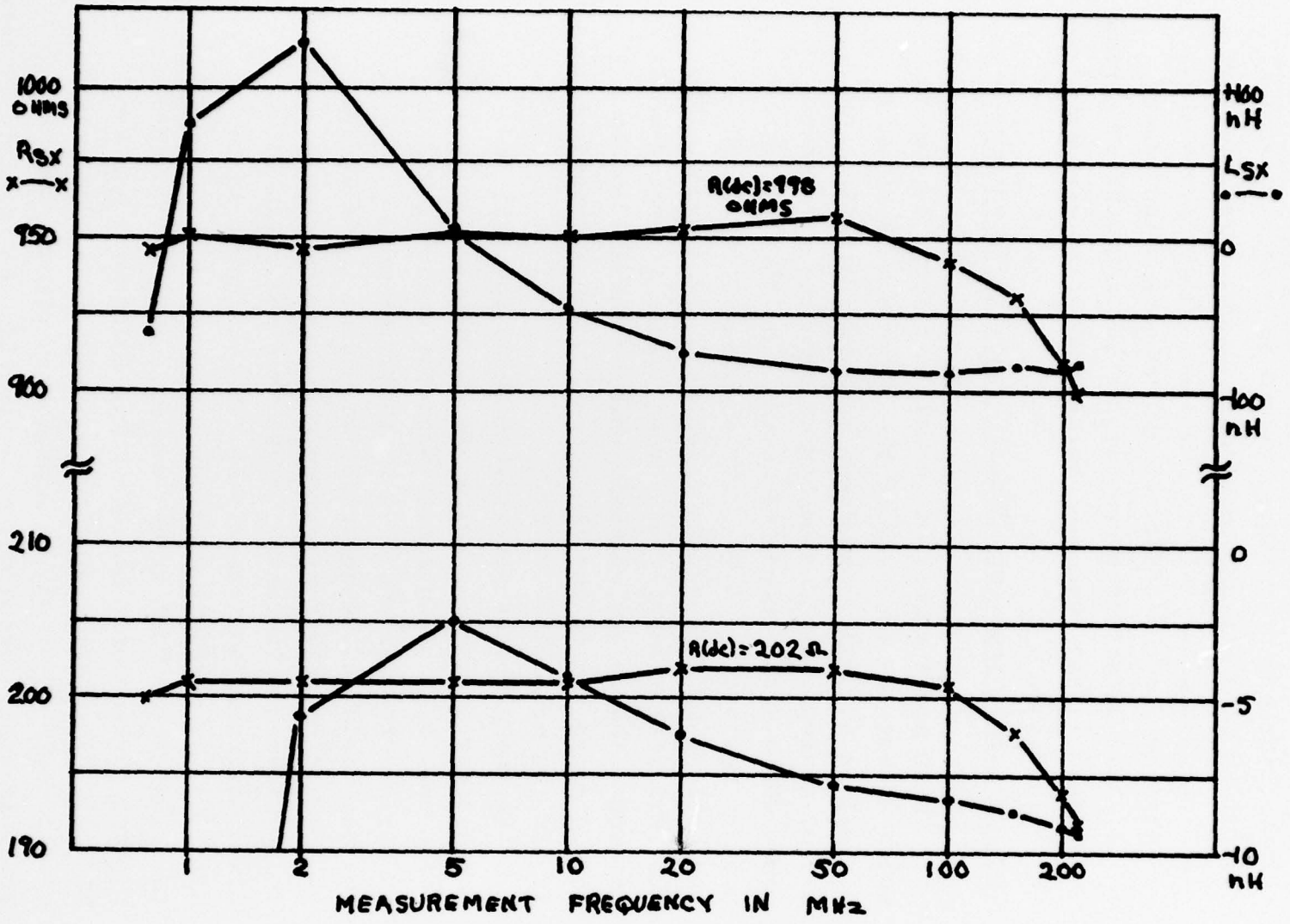


FIGURE 4.7.4.3 MEASURED VALUES OF THICK FILM RESISTORS

4.7.5 Measured Values of Ceramic Chip Capacitators

Figures 4.7.5.1, 4.7.5.2, and 4.7.5.3 are plots versus frequency of measured values of effective series capacitance and resistance of ceramic chip capacitors of 2 and 30 pF nominal values. Measured values shown include corrections for the effect of 0.9 nH series inductance in C2, 0.71 nH series inductance in C6, and 2.08 nH series inductance in the "unknown" terminals of the circuit shown in Figure 4.2.1.

4.8 Optimum Corrections for Circuit Parasitic Impedances

There are a number of parasitic circuit impedance which affect the accuracy of the measurements of this as well as any other impedance measuring circuit. The use of microcircuit components extends the frequency range where stray impedance become significant, but the need to measure relatively low impedances, makes the connections to the unknown of critical importance. The most critical internal stray capacitance is that from R1 to ground and in our assembly this is guarded out by a shield connected to the input of R1 which surrounds both it and its connection to C1.

In the previous section, we chose to limit the corrections to those required for three fixed-valued inductors, 2.08 nH in series with the unknown, 0.9 nH in series with C2, and 0.71 nH in series with C6. It is not certain that the number or values of these strays is optimum for the application, but they do seem to produce reasonable indicated values when measuring both fixed resistors and capacitors. The values seem to be high for the physical configuration. We do consider the right-angle turn in the connection to the unknown contact particularly bad for stray inductance and the planar configuration proposed by ERADCOM to have considerable merit if it can be implemented without increasing internal stray impedances or destroying the required isolation. The need to accommodate multiple series loading capacitors

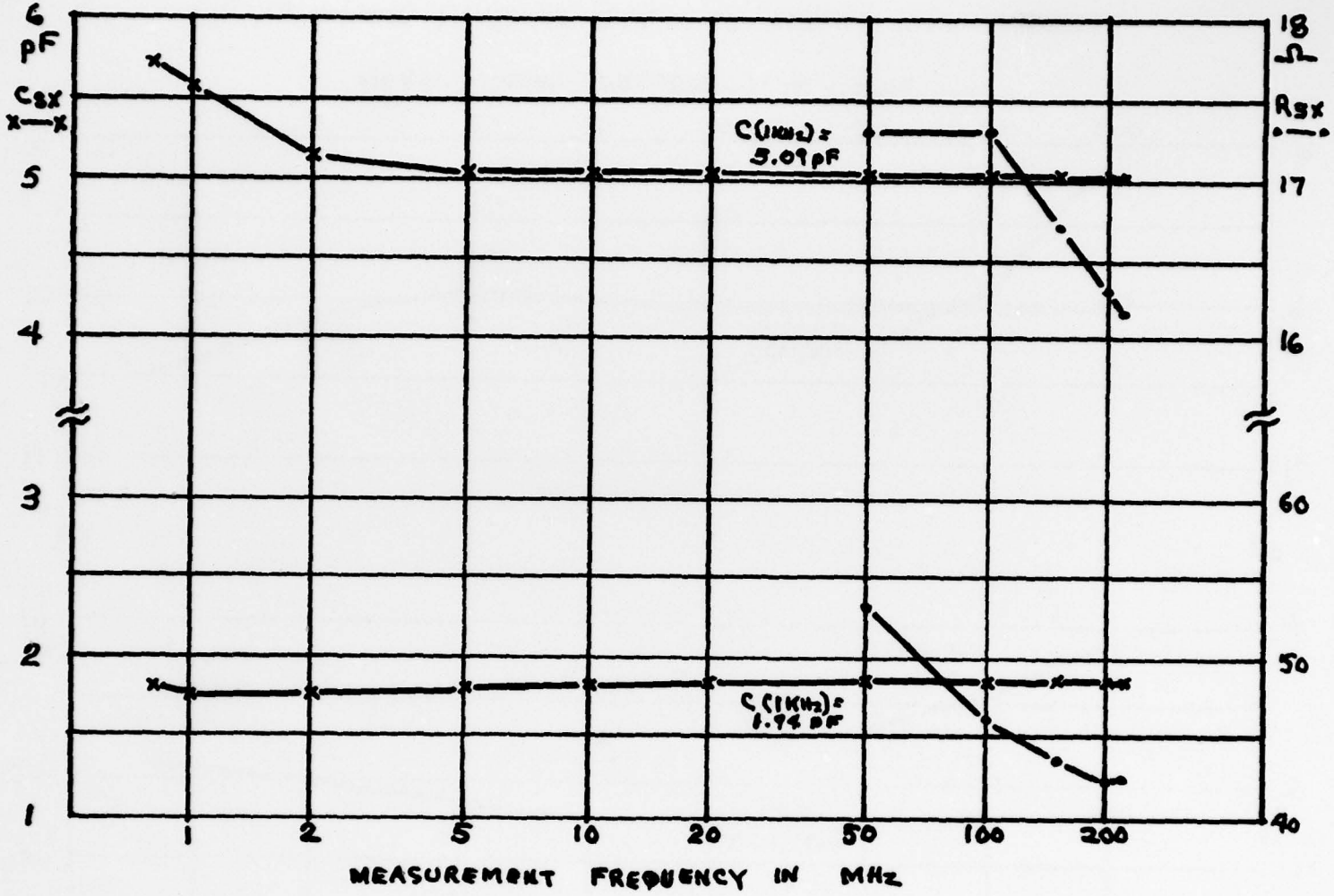


FIGURE 4.7.5.1 MEASURED VALUES OF CERAMIC CHIP CAPACITORS

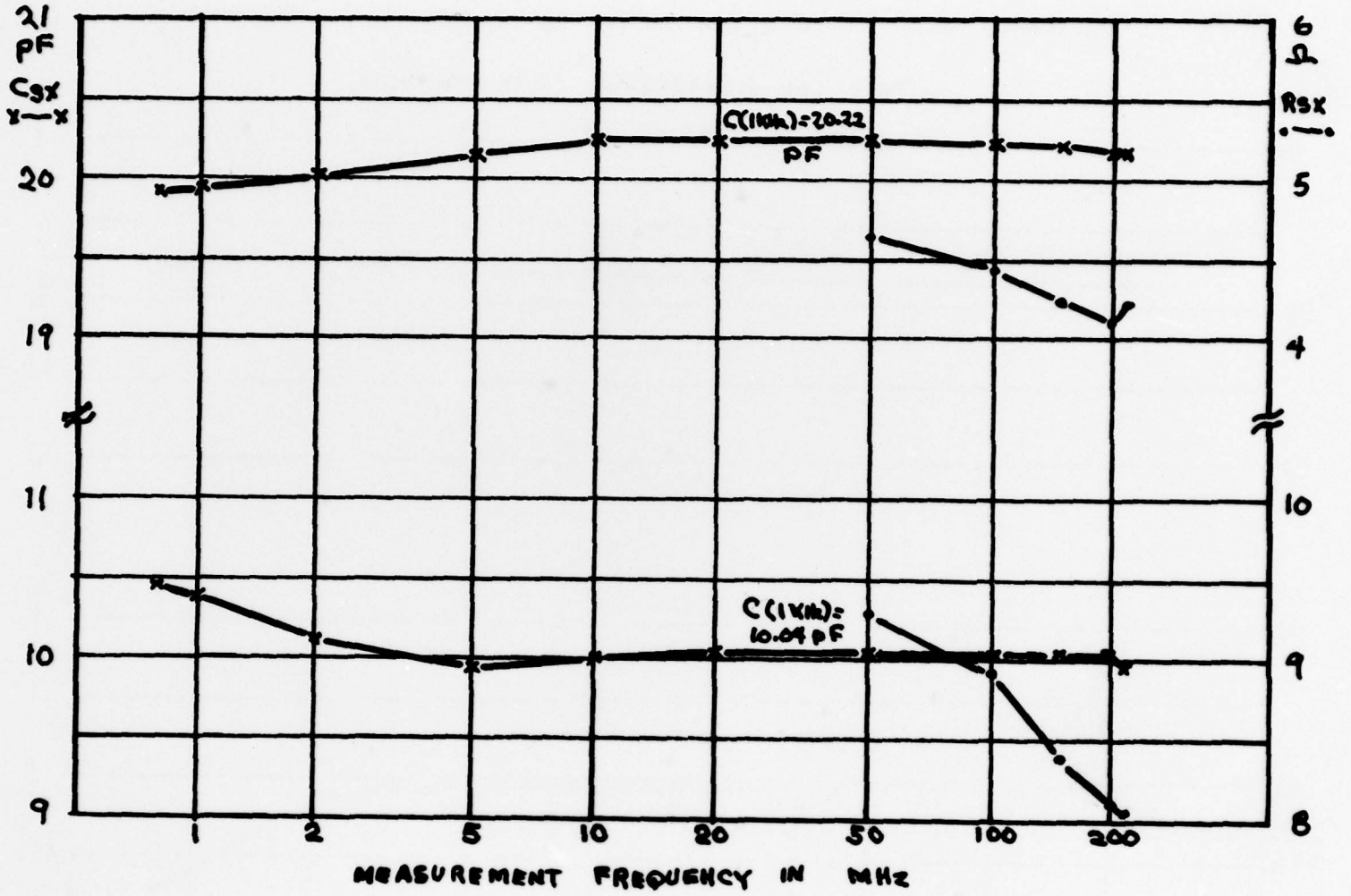


FIGURE 4.7.5.2 MEASURED VALUES OF CERAMIC CHIP CAPACITORS

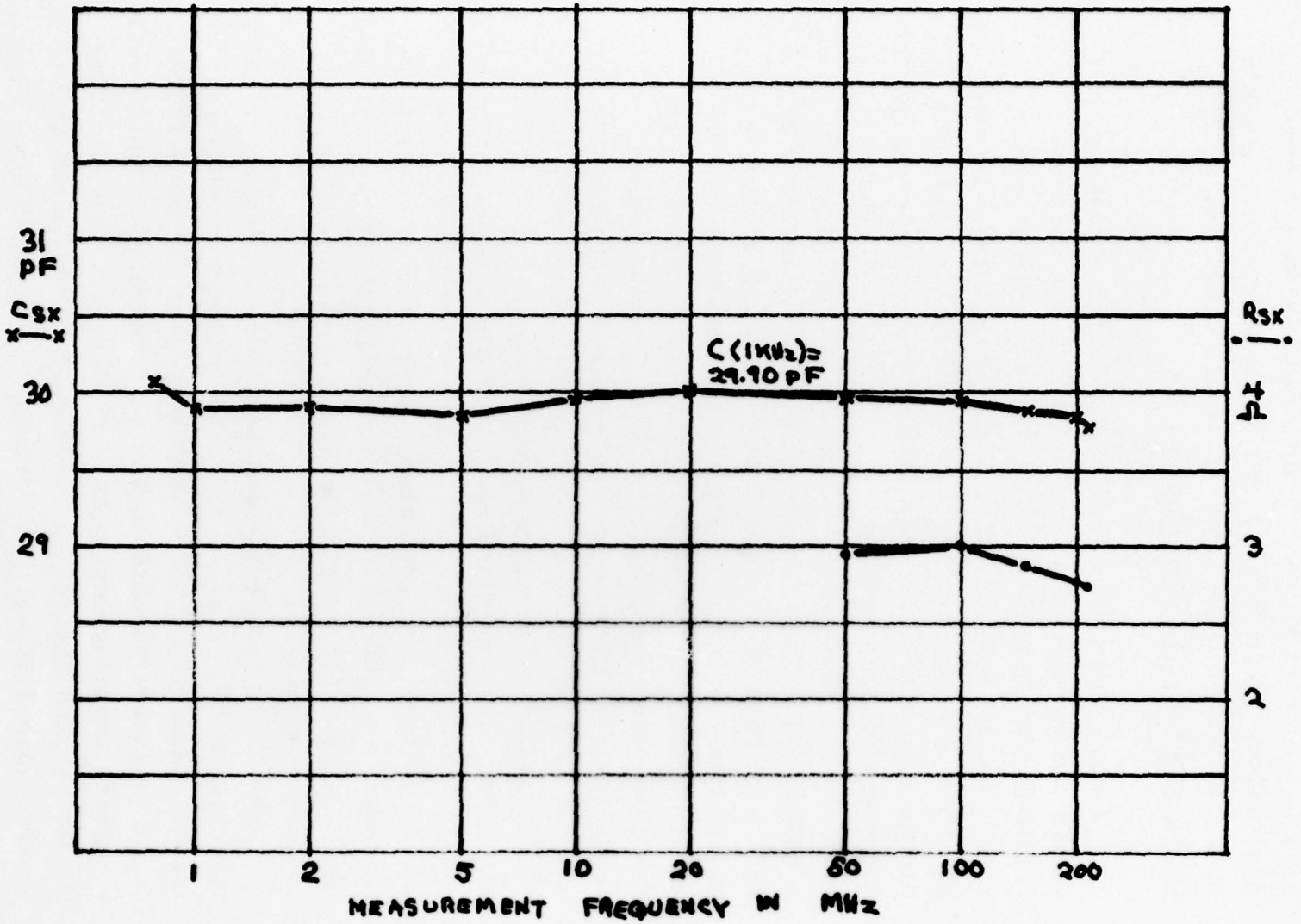


FIGURE 4.7.5.3 MEASURED VALUES OF CERAMIC CHIP CAPACITORS

will add additional series inductance with any configuration, and certainly the screw-mounted-replaceable contacts should be avoided if at all possible.

4.9 Conclusions and Recommendations

Abrupt junction varactor diodes are amazingly stable and mathematically characterizable devices. Suitably low-loss diode chips for the wide frequency range desired have somewhat limited capacitance range, but their use as electrically controllable balancing elements in a microcircuit bridge provides the performance necessary for measurement of parameters of quartz resonators. Since the reactance range is severely limited at the lower frequencies, the suitability of such a bridge for general impedance measurements is questionable. It is practical to compensate for the normal varactor-diode temperature characteristics by the insertion of a properly scaled linear-versus-temperature dc offset voltage in series with the applied control voltages over a temperature range of -50 to +105^{o}C and obtain accuracies within 0.1 pF in terms of balancing capacitance values. Whether this will permit resolution to the desired accuracy of parallel resistance values as high as 20,000 ohms with bridge values suitable for measuring down to 2 ohms is undetermined, but certainly performance for values up to 1,000 ohms or so should be quite adequate.

There seem to be serious performance problems with attaching diode chips to the other circuit components without destroying their inherently good characteristics. It is essential to produce low resistance bonds which will withstand repeated temperature cycling without affecting the dc reverse leakage of the chips. There seems to be considerable difficulty in attaching them with low-temperature solder without destroying their performance.

Perhaps this is due to faulty units, but this is not certain.

The design of a sealed assembly that will withstand repeated temperature cycling is considered a critical undertaking. Complete avoidance of solder in the assembly is highly recommended. The use of metals with low temperature coefficients of expansion is essential, if ceramic is to be bonded to rigid assemblies, but the electrical properties of such metals are far from ideal, requiring heavy plating. A completely ceramic structure using heavy metalization where required for conductivity, should seriously be considered. Conductive structural closures can perhaps best be made by cold welding metallic flanges.

It is felt that a reasonable number of corrections for stray impedance elements in the bridge can be incorporated in a desk-calculator readout system, which can also be used to produce readout in terms of the desired parameters. Accuracy of the readout can no doubt be improved by a number of averaging and calibrating techniques, using software in the calculator/controller if desired.

5.0 OVERALL CONCLUSIONS

An Automatic Microcircuit Bridge system for measuring quartz-crystal resonators can be assembled with a number of specialized modular instruments which will perform the necessary measurements to characterize these resonators in terms of their equivalent circuit parameters, C_o, C_1, L_1, Q_o, f_r, and R_r, from computations automatically performed by a desk calculator/controller. With the addition of an environmental temperature control system, these parameter values can be displayed as a function of temperature and time. The accuracy of the measurements is dependent not only on the ability to minimize the stray parameters in and the stability of the bridge, but on the ability of the computations to include corrections for errors and possibly calibration data. The performance achievable by the later process remains to be determined, but it is expected that considerable improvements in accuracy can be obtained once a reliable operating system is assembled.

The success of the system depends on a stable Microcircuit Bridge assembly that can repeatably make reliable, well defined connections to the device under test, and withstand the environmental changes imposed on that device with predictable effects on the impedance values indicated. The frequency range over which the parasitic elements can be characterized depends on how well these elements can be controlled. It is expected that the frequency range of 0.8 to 220 MHz can be attained with the desired performance accuracy.